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Attorneys for Defendant
PATRIOT SCIENTIFIC CORPORATION

UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN JOSE DIVISION

ACER, INC., ACER AMERICA
CORPORATION and GATEWAY, INC.,

Plaintiff,

v.

TECHNOLOGY PROPERTIES
LIMITED, PATRIOT SCIENTIFIC
CORPORATION, and ALLIACENSE
LIMITED,

Defendants.

Case No. 5:08-cv-00877 JF

**DECLARATION OF JOHN L. COOPER IN
SUPPORT OF MOTION TO DISMISS AND
TO TRANSFER**

Date: August 1, 2008
Time: 9:00 a.m.
Dept: Courtroom 3, 5th Floor
Before: Honorable Jeremy Fogel

1 I, John L. Cooper, declare the following:

2 1. I am an attorney licensed to practice law in the State of California and am a partner
3 with the firm of Farella Braun & Martel LLP, counsel for Defendants Technology Properties
4 Limited ("TPL") and Alliacense Limited in this action. I have personal knowledge of the facts set
5 forth below and, if called upon to do so, could and would testify competently thereto.

6 2. On April 25, 2008, TPL filed a complaint in the Eastern District of Texas alleging
7 that plaintiffs infringe the MMP patents. These patents include U.S. Patent Nos. 5,809,336 ("the
8 '336 patent"), 5,784,584 ("the '584 patent"), 5,440,749 ("the '749 patent"), and 6,598,148 ("the
9 '148 patent"). TPL has sought to have this action assigned to Judge Ward.

10 3. Attached hereto as Exhibit A is a true and correct copy of *Technology Properties*
11 *Limited v. Fujitsu et al* Complaint for Patent Infringement, filed on October 24, 2005 in the
12 Eastern District of Texas, Marshall Division.

13 4. Attached hereto as Exhibit B is a true and correct copy of *Technology Properties*
14 *Limited v. Fujitsu et al*, Notice of Filing Defendants' Technology Tutorial filed on April 25, 2007
15 in the Eastern District of Texas, Marshall Division.

16 5. Attached hereto as Exhibit C is a true and correct copy of *Technology Properties*
17 *Limited v. Fujitsu et al*, Memorandum Opinion and Order filed on June 15, 2007 in the Eastern
18 District of Texas, Marshall Division, Docket No. 259.

19 6. Attached hereto as Exhibit D is a true and correct copy of Plaintiffs' Amended
20 Notice of Appeal, filed on October 22, 2007 in the Eastern District of Texas, Marshall Division,
21 Docket No. 350.

22 7. Attached hereto as Exhibit E is a true and correct copy of ARM, Ltd.'s First
23 Amended Answer to Plaintiff's Second Amended Complaint, filed on February 16, 2007 in the
24 Eastern District of Texas, Marshall Division, Docket No. 203.

25 8. I am reliably informed that Charles Moore, the lead inventor listed on the MMP
26 patents, is a consultant for TPL.

27

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EXHIBIT A

**TO THE DECLARATION OF JOHN L. COOPER IN
SUPPORT OF MOTION TO DISMISS AND TO
TRANSFER**

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

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Technology Properties Limited, Inc.,

Plaintiff,

vs.

Fujitsu Limited, Fujitsu General America, Inc.,
Fujitsu Computer Products of America, Inc.,
Fujitsu Computer Systems Corp., Fujitsu
Microelectronics America, Inc., Fujitsu Ten
Corporation of America, Matsushita Electrical
Industrial Co., Ltd., Panasonic Corporation of
North America, JVC Americas Corporation,
NEC Corporation, NEC Electronics America,
Inc., NEC America, Inc., NEC Display
Solutions of America, Inc., NEC Solutions
America, Inc., NEC Unified Solutions, Inc.,
Toshiba Corporation, Toshiba America, Inc.,
Toshiba America Electronic Components, Inc.,
Toshiba America Information Systems, Inc. and
Toshiba America Consumer Products, LLC,

Defendants.

Civil Action No.

2-05 CV-494

Jury Trial Demanded

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Technology Properties Limited, Inc., for its complaint against defendants Fujitsu Limited, Fujitsu General America, Inc., Fujitsu Computer Products of America, Inc., Fujitsu Computer Systems Corp., Fujitsu Microelectronics America, Inc., Fujitsu Ten Corporation of America, Matsushita Electrical Industrial Co., Ltd., Panasonic Corporation of North America, JVC Americas Corporation, NEC Corporation, NEC Electronics America, Inc., NEC America, Inc., NEC Display Solutions of America, Inc., NEC Solutions America, Inc., NEC Unified Solutions, Inc., Toshiba Corporation, Toshiba America, Inc., Toshiba America Electronic Components, Inc., Toshiba America Information Systems, Inc. and Toshiba America Consumer Products, LLC, alleges:

THE PARTIES

1. Plaintiff Technology Properties Limited, Inc. ("TPL"), is a corporation duly organized and existing under the laws of the State of California, and maintains its principal place of business in San Jose, California.

2. TPL is informed and believes, and on the basis of such information and belief alleges, that defendant Fujitsu, Ltd. ("Fujitsu"), is a corporation organized and existing under the laws of the Country of Japan, and maintains its principal place of business at Shiodome City Center, 1-5-2 Higashi-Shimbashi, Minato-ku, Tokyo 105-7123, Japan.

3. TPL is informed and believes, and on the basis of such information and belief alleges, that defendant Fujitsu General America, Inc. ("Fujitsu General"), is a corporation organized and existing under the laws of the State of Delaware, and maintains its principal place of business at 353 Route 46 West, Fairfield, NJ 07004.

4. TPL is informed and believes, and on the basis of such information and belief alleges, that defendant Fujitsu Computer Products of America, Inc. ("Fujitsu Computer Products"), is a corporation organized and existing under the laws of the State of California and maintains its principal place of business at 2904 Orchard Parkway, San Jose, CA 95134.

5. TPL is informed and believes, and on the basis of such information and belief alleges, that defendant Fujitsu Computer Systems Corp. ("Fujitsu Computer Systems") is a corporation organized and existing under the laws of the State of California, and maintains its principal place of business at 1250 East Arquez Avenue M/S 124, Sunnyvale, CA 94085.

6. TPL is informed and believes, and on the basis of such information and belief alleges, that defendant Fujitsu Microelectronics America, Inc. ("Fujitsu Microelectronics"), is a corporation organized and existing under the laws of the State of California, and maintains its principal place of business at 1250 East Arquez Avenue M/S 333, Sunnyvale, CA 94088-3470.

7. TPL is informed and believes, and on the basis of such information and belief alleges, that defendant Fujitsu Ten Corporation of America ("Fujitsu Ten"), is a corporation

organized and existing under the laws of the State of California, and maintains its principal place of business at 19600 South Vermont Avenue, Torrance, CA 90502.

8. TPL is informed and believes, and on the basis of such information and belief alleges, that defendant Matsushita Electrical Industrial Co., Ltd. ("Matsushita"), is a corporation organized and existing under the laws of the Country of Japan, and maintains its principal place of business at 1006, Kadoma, Kadoma City, Osaka 571-8501, Japan.

9. TPL is informed and believes, and on the basis of such information and belief alleges, that defendant Panasonic Corporation of North America ("Panasonic") is a corporation organized and existing under the laws of the State of Delaware, and maintains its principal place of business at One Panasonic Way, Secaucus, NJ 07094.

10. TPL is informed and believes, and on the basis of such information and belief alleges, that defendant JVC Americas Corporation ("JVC") is a corporation organized and existing under the laws of the State of Delaware, and maintains its principal place of business at 1700 Valley Road, Wayne, NJ 07470.

11. TPL is informed and believes, and on the basis of such information and belief alleges, that defendant NEC Corporation ("NEC") is a corporation organized and existing under the laws of the Country of Japan, and maintains its principal place of business at 7-1, Shiba 5-chome, Minato-ku, Tokyo 108-8001.

12. TPL is informed and believes, and on the basis of such information and belief alleges, that defendant NEC Electronics America, Inc. ("NEC Electronics") is a corporation organized and existing under the laws of the State of California, and maintains its principal place of business at 2880 Scott Boulevard, Santa Clara, CA 95050-2554.

13. TPL is informed and believes, and on the basis of such information and belief alleges, that defendant NEC America, Inc. ("NEC America"), is a corporation organized and existing under the laws of the State of New York, and maintains its principal place of business at 6555 North State Highway 161, Irving, Texas 75039.

14. TPL is informed and believes, and on the basis of such information and belief alleges, that defendant NEC Display Solutions of America, Inc., ("NEC Display") is a

corporation organized and existing under the laws of the State of Delaware, and maintains its principal place of business at 500 Park Boulevard, Suite 1100, Itasca, IL 60143.

15. TPL is informed and believes, and on the basis of such information and belief alleges, that defendant NEC Solutions America, Inc. ("NEC Solutions"), is a corporation organized and existing under the laws of the State of Delaware, and maintains its principal place of business at 10850 Gold Center Drive #200, Ranch Cordova, CA 95670.

16. TPL is informed and believes, and on the basis of such information and belief alleges, that defendant NEC Unified Solutions, Inc. ("NEC Unified"), is a corporation organized and existing under the laws of the State of Nevada, and maintains its principal place of business at 6555 North State Highway 161, Irving, Texas 75039.

17. TPL is informed and believes, and on the basis of such information and belief alleges, that defendant Toshiba Corporation ("Toshiba") is a corporation organized and existing under the laws of the Country of Japan, and maintains its principal place of business at 1-1, Shibaura 1-chome, Minato-ku, Tokyo 105-8001, Japan.

18. TPL is informed and believes, and on the basis of such information and belief alleges, that defendant Toshiba America, Inc. ("Toshiba America"), is a corporation organized and existing under the laws of the State of Delaware, and maintains its principal place of business at 1251 Avenue of the Americas, Suite 4100, New York, NY 10020.

19. TPL is informed and believes, and on the basis of such information and belief alleges, that defendant Toshiba America Electronic Components, Inc. ("Toshiba Electronic"), is a corporation organized and existing under the laws of the State of California, and maintains its principal place of business at 19900 MacArthur Boulevard, Suite 400, Irvine, CA 92612.

20. TPL is informed and believes, and on the basis of such information and belief alleges, that defendant Toshiba America Information Systems, Inc. ("Toshiba Information"), is a corporation organized and existing under the laws of the State of California, and maintains its principal place of business at 9740 Irvine Boulevard, Irvine, CA 92618.

21. TPL is informed and believes, and on the basis of such information and belief alleges, that defendant Toshiba America Consumer Products, LLC ("Toshiba Consumer"), is a

limited liability corporation organized and existing under the laws of the State of New Jersey, and maintains its principal place of business at 82 Totowa Road, Wayne, NJ 07470.

JURISDICTION AND VENUE

22. The court has subject matter jurisdiction pursuant to 28 U.S.C. §§1331 and 1338(a) because this action arises under the patent laws of the United States, 35 U.S.C. §§1 *et seq.*

23. Venue is proper in this district as to defendants, and each of them, pursuant to 28 U.S.C. §§1391(b),(c),(d) and 1400(b) in that defendants have done business in this district, have committed acts of infringement in this district, and continue to commit acts of infringement in this district.

THE PATENTS

24. On July 22, 2003, United States Patent No. 6,598,148 ("the '148 patent") was duly and legally issued for an invention entitled "High Performance Microprocessor Having Variable Speed System Clock." A true and correct copy of the '148 patent is attached hereto as Exhibit A.

25. On September 15, 1998, United States Patent No. 5,809,336 ("the '336 patent") was duly and legally issued for an invention entitled "High Performance Microprocessor Having Variable Speed System Clock." A true and correct copy of the '336 patent is attached hereto as Exhibit B.

26. On July 21, 1998, United States Patent No. 5,784,584 ("the '584 patent") was duly and legally issued for an invention entitled "High Performance Microprocessor Using Instructions That Operate Within Instruction Groups." A true and correct copy of the '584 patent is attached hereto as Exhibit C.

27. TPL is an owner of the right, title and interest to the '148 patent, the '336 patent, and the '584 patent (collectively, "the patents-in-suit"), has the exclusive right to enforce and license the patents-in-suit, and has standing to sue.

INFRINGEMENT BY FUJITSU

28. Fujitsu has infringed and continues to infringe the patents-in-suit, and each of them, by its manufacture, use, sale, importation, and/or offer for sale of infringing products including Fujitsu microprocessors and microcontrollers and products embodying Fujitsu microprocessors and microcontrollers; and its contributing to and inducement of others to manufacture, use, sell, import, and/or offer for sale infringing products. Fujitsu is liable for its infringement of the patents-in-suit, and each of them, pursuant to 35 U.S.C. § 271.

29. Fujitsu General has infringed and continues to infringe the patents-in-suit, and each of them, by its manufacture, use, sale, importation, and/or offer for sale of infringing products including Fujitsu microprocessors and microcontrollers and products embodying Fujitsu microprocessors and microcontrollers; and its contributing to and inducement of others to manufacture, use, sell, import, and/or offer for sale infringing products. Fujitsu General is liable for its infringement of the patents-in-suit, and each of them, pursuant to 35 U.S.C. § 271.

30. Fujitsu Computer Products has infringed and continues to infringe the patents-in-suit, and each of them, by its manufacture, use, sale, importation, and/or offer for sale of infringing products including Fujitsu microprocessors and microcontrollers and products embodying Fujitsu microprocessors and microcontrollers; and its contributing to and inducement of others to manufacture, use, sell, import, and/or offer for sale infringing products. Fujitsu Computer Products is liable for its infringement of the patents-in-suit, and each of them, pursuant to 35 U.S.C. § 271.

31. Fujitsu Computer Systems has infringed and continues to infringe the patents-in-suit, and each of them, by its manufacture, use, sale, importation, and/or offer for sale of infringing products including Fujitsu microprocessors and microcontrollers and products embodying Fujitsu microprocessors and microcontrollers; and its contributing to and inducement of others to manufacture, use, sell, import, and/or offer for sale infringing products. Fujitsu Computer Systems is liable for its infringement of the patents-in-suit, and each of them, pursuant to 35 U.S.C. § 271.

32. Fujitsu Microelectronics has infringed and continues to infringe the patents-in-suit, and each of them, by its manufacture, use, sale, importation, and/or offer for sale of infringing products including Fujitsu microprocessors and microcontrollers and products embodying Fujitsu microprocessors and microcontrollers; and its contributing to and inducement of others to manufacture, use, sell, import, and/or offer for sale infringing products. Fujitsu Microelectronics is liable for its infringement of the patents-in-suit, and each of them, pursuant to 35 U.S.C. § 271.

33. Fujitsu Ten has infringed and continues to infringe the patents-in-suit, and each of them, by its manufacture, use, sale, importation, and/or offer for sale of infringing products including Fujitsu microprocessors and microcontrollers and products embodying Fujitsu microprocessors and microcontrollers; and its contributing to and inducement of others to manufacture, use, sell, import, and/or offer for sale infringing products. Fujitsu Ten is liable for its infringement of the patents-in-suit, and each of them, pursuant to 35 U.S.C. § 271.

34. Fujitsu's acts of infringement have caused damage to plaintiff and plaintiff is entitled to recover from Fujitsu the damages sustained by it as a result of Fujitsu's wrongful acts in an amount subject to proof at trial. Fujitsu's infringement of plaintiff's rights under the patents-in-suit will continue to damage plaintiff, causing irreparable harm for which there is no adequate remedy at law unless enjoined by this Court.

35. Fujitsu General's acts of infringement have caused damage to plaintiff and plaintiff is entitled to recover from Fujitsu the damages sustained by it as a result of Fujitsu's wrongful acts in an amount subject to proof at trial. Fujitsu General's infringement of plaintiff's rights under the patents-in-suit will continue to damage plaintiff, causing irreparable harm for which there is no adequate remedy at law unless enjoined by this Court.

36. Fujitsu Computer Products' acts of infringement have caused damage to plaintiff and plaintiff is entitled to recover from Fujitsu Computer Products the damages sustained by it as a result of Fujitsu's wrongful acts in an amount subject to proof at trial. Fujitsu Computer Products' infringement of plaintiff's rights under the patents-in-suit will continue to damage

plaintiff, causing irreparable harm for which there is no adequate remedy at law unless enjoined by this Court.

37. Fujitsu Computer Systems' acts of infringement have caused damage to plaintiff and plaintiff is entitled to recover from Fujitsu Computer Systems the damages sustained by it as a result of Fujitsu's wrongful acts in an amount subject to proof at trial. Fujitsu Computer Systems' infringement of plaintiff's rights under the patents-in-suit will continue to damage plaintiff, causing irreparable harm for which there is no adequate remedy at law unless enjoined by this Court.

38. Fujitsu Microelectronics' acts of infringement have caused damage to plaintiff and plaintiff is entitled to recover from Fujitsu Microelectronis the damages sustained by it as a result of Fujitsu Microelectronics' wrongful acts in an amount subject to proof at trial. Fujitsu Microelectronics' infringement of plaintiff's rights under the patents-in-suit will continue to damage plaintiff, causing irreparable harm for which there is no adequate remedy at law unless enjoined by this Court.

39. Fujitsu Ten's acts of infringement have caused damage to plaintiff and plaintiff is entitled to recover from Fujitsu Ten the damages sustained by it as a result of Fujitsu Ten's wrongful acts in an amount subject to proof at trial. Fujitsu Ten's infringement of plaintiff's rights under the patents-in-suit will continue to damage plaintiff, causing irreparable harm for which there is no adequate remedy at law unless enjoined by this Court.

40. Upon information and belief, Fujitsu's infringement of the patents-in-suit is willful and deliberate, entitling plaintiff to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

41. Upon information and belief, Fujitsu General's infringement of the patents-in-suit is willful and deliberate, entitling plaintiff to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

42. Upon information and belief, Fujitsu Computer Products' infringement of the patents-in-suit is willful and deliberate, entitling plaintiff to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285

43. Upon information and belief, Fujitsu Computer Systems' infringement of the patents-in-suit is willful and deliberate, entitling plaintiff to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

44. Upon information and belief, Fujitsu Microelectronic's infringement of the patents-in-suit is willful and deliberate, entitling plaintiff to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

45. Upon information and belief, Fujitsu Ten's infringement of the patents-in-suit is willful and deliberate, entitling plaintiff to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

INFRINGEMENT BY MATSUSHITA

46. Matsushita has infringed and continues to infringe the patents-in-suit, and each of them, by its manufacture, use, sale, importation, and/or offer for sale of infringing products including Matsushita microprocessors and microcontrollers and products embodying Matsushita microprocessors and microcontrollers; and its contributing to and inducement of others to manufacture, use, sell, import, and/or offer for sale infringing products. Matsushita is liable for its infringement of the patents-in-suit, and each of them, pursuant to 35 U.S.C. § 271.

47. Panasonic has infringed and continues to infringe the patents-in-suit, and each of them, by its manufacture, use, sale, importation, and/or offer for sale of infringing products including Matsushita microprocessors and microcontrollers and products embodying Matsushita microprocessors and microcontrollers; and its contributing to and inducement of others to manufacture, use, sell, import, and/or offer for sale infringing products. Panasonic is liable for its infringement of the patents-in-suit, and each of them, pursuant to 35 U.S.C. § 271.

48. JVC has infringed and continues to infringe the patents-in-suit, and each of them, by its manufacture, use, sale, importation, and/or offer for sale of infringing products including Matsushita microprocessors and microcontrollers and products embodying Matsushita microprocessors and microcontrollers; and its contributing to and inducement of others to manufacture, use, sell, import, and/or offer for sale infringing products. JVC is liable for its infringement of the patents-in-suit, and each of them, pursuant to 35 U.S.C. § 271.

49. Matsushita's acts of infringement have caused damage to plaintiff and plaintiff is entitled to recover from Matsushita the damages sustained by it as a result of Matsushita's wrongful acts in an amount subject to proof at trial. Matsushita's infringement of plaintiff's rights under the patents-in-suit will continue to damage plaintiff, causing irreparable harm for which there is no adequate remedy at law unless enjoined by this Court.

50. Panasonic's acts of infringement have caused damage to plaintiff and plaintiff is entitled to recover from Panasonic the damages sustained by it as a result of Panasonic's wrongful acts in an amount subject to proof at trial. Panasonic's infringement of plaintiff's rights under the patents-in-suit will continue to damage plaintiff, causing irreparable harm for which there is no adequate remedy at law unless enjoined by this Court.

51. JVC's acts of infringement have caused damage to plaintiff and plaintiff is entitled to recover from Matsushita the damages sustained by it as a result of JVC's wrongful acts in an amount subject to proof at trial. JVC's infringement of plaintiff's rights under the patents-in-suit will continue to damage plaintiff, causing irreparable harm for which there is no adequate remedy at law unless enjoined by this Court.

52. Upon information and belief, Matsushita's infringement of the patents-in-suit is willful and deliberate, entitling plaintiff to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

53. Upon information and belief, Panasonic's infringement of the patents-in-suit is willful and deliberate, entitling plaintiff to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

54. Upon information and belief, JVC's infringement of the patents-in-suit is willful and deliberate, entitling plaintiff to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

INFRINGEMENT BY NEC

55. NEC has infringed and continues to infringe the patents-in-suit, and each of them, by its manufacture, use, sale, importation, and/or offer for sale of infringing products including NEC microprocessors and microcontrollers and products embodying NEC microprocessors and

microcontrollers; and its contributing to and inducement of others to manufacture, use, sell, import, and/or offer for sale infringing products. NEC is liable for its infringement of the patents-in-suit, and each of them, pursuant to 35 U.S.C. § 271.

56. NEC Electronics has infringed and continues to infringe the patents-in-suit, and each of them, by its manufacture, use, sale, importation, and/or offer for sale of infringing products including NEC microprocessors and microcontrollers and products embodying NEC microprocessors and microcontrollers; and its contributing to and inducement of others to manufacture, use, sell, import, and/or offer for sale infringing products. NEC Electronics is liable for its infringement of the patents-in-suit, and each of them, pursuant to 35 U.S.C. § 271.

57. NEC America has infringed and continues to infringe the patents-in-suit, and each of them, by its manufacture, use, sale, importation, and/or offer for sale of infringing products including NEC microprocessors and microcontrollers and products embodying NEC microprocessors and microcontrollers; and its contributing to and inducement of others to manufacture, use, sell, import, and/or offer for sale infringing products. NEC America is liable for its infringement of the patents-in-suit, and each of them, pursuant to 35 U.S.C. § 271.

58. NEC Display has infringed and continues to infringe the patents-in-suit, and each of them, by its manufacture, use, sale, importation, and/or offer for sale of infringing products including NEC microprocessors and microcontrollers and products embodying NEC microprocessors and microcontrollers; and its contributing to and inducement of others to manufacture, use, sell, import, and/or offer for sale infringing products. NEC Display is liable for its infringement of the patents-in-suit, and each of them, pursuant to 35 U.S.C. § 271.

59. NEC Solutions has infringed and continues to infringe the patents-in-suit, and each of them, by its manufacture, use, sale, importation, and/or offer for sale of infringing products including NEC microprocessors and microcontrollers and products embodying NEC microprocessors and microcontrollers; and its contributing to and inducement of others to manufacture, use, sell, import, and/or offer for sale infringing products. NEC Solutions is liable for its infringement of the patents-in-suit, and each of them, pursuant to 35 U.S.C. § 271.

60. NEC Unified has infringed and continues to infringe the patents-in-suit, and each of them, by its manufacture, use, sale, importation, and/or offer for sale of infringing products including NEC microprocessors and microcontrollers and products embodying NEC microprocessors and microcontrollers; and its contributing to and inducement of others to manufacture, use, sell, import, and/or offer for sale infringing products. NEC Unified is liable for its infringement of the patents-in-suit, and each of them, pursuant to 35 U.S.C. § 271.

61. NEC's acts of infringement have caused damage to plaintiff and plaintiff is entitled to recover from NEC the damages sustained by it as a result of NEC's wrongful acts in an amount subject to proof at trial. NEC's infringement of plaintiff's rights under the patents-in-suit will continue to damage plaintiff, causing irreparable harm for which there is no adequate remedy at law unless enjoined by this Court.

62. NEC Electronics' acts of infringement have caused damage to plaintiff and plaintiff is entitled to recover from NEC Electronics the damages sustained by it as a result of NEC Electronics' wrongful acts in an amount subject to proof at trial. NEC Electronics' infringement of plaintiff's rights under the patents-in-suit will continue to damage plaintiff, causing irreparable harm for which there is no adequate remedy at law unless enjoined by this Court.

63. NEC America's acts of infringement have caused damage to plaintiff and plaintiff is entitled to recover from NEC America the damages sustained by it as a result of NEC America's wrongful acts in an amount subject to proof at trial. NEC America's infringement of plaintiff's rights under the patents-in-suit will continue to damage plaintiff, causing irreparable harm for which there is no adequate remedy at law unless enjoined by this Court.

64. NEC Display's acts of infringement have caused damage to plaintiff and plaintiff is entitled to recover from NEC Display the damages sustained by it as a result of NEC Display's wrongful acts in an amount subject to proof at trial. NEC Display's infringement of plaintiff's rights under the patents-in-suit will continue to damage plaintiff, causing irreparable harm for which there is no adequate remedy at law unless enjoined by this Court.

65. NEC Solutions' acts of infringement have caused damage to plaintiff and plaintiff is entitled to recover from NEC Solutions the damages sustained by it as a result of NEC Solutions' wrongful acts in an amount subject to proof at trial. NEC Solutions' infringement of plaintiff's rights under the patents-in-suit will continue to damage plaintiff, causing irreparable harm for which there is no adequate remedy at law unless enjoined by this Court.

66. NEC Unified's acts of infringement have caused damage to plaintiff and plaintiff is entitled to recover from NEC Unified the damages sustained by it as a result of NEC Unified's wrongful acts in an amount subject to proof at trial. NEC Unified's infringement of plaintiff's rights under the patents-in-suit will continue to damage plaintiff, causing irreparable harm for which there is no adequate remedy at law unless enjoined by this Court.

67. Upon information and belief, NEC's infringement of the patents-in-suit is willful and deliberate, entitling plaintiff to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

68. Upon information and belief, NEC Electronics' infringement of the patents-in-suit is willful and deliberate, entitling plaintiff to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

69. Upon information and belief, NEC America's infringement of the patents-in-suit is willful and deliberate, entitling plaintiff to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

70. Upon information and belief, NEC Display's infringement of the patents-in-suit is willful and deliberate, entitling plaintiff to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

71. Upon information and belief, NEC Solutions' infringement of the patents-in-suit is willful and deliberate, entitling plaintiff to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

72. Upon information and belief, NEC Unified's infringement of the patents-in-suit is willful and deliberate, entitling plaintiff to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

INFRINGEMENT BY TOSHIBA

73. Toshiba has infringed and continues to infringe the patents-in-suit, and each of them, by its manufacture, use, sale, importation, and/or offer for sale of infringing products including Toshiba microprocessors and microcontrollers and products embodying Toshiba microprocessors and microcontrollers; and its contributing to and inducement of others to manufacture, use, sell, import, and/or offer for sale infringing products. Toshiba is liable for its infringement of the patents-in-suit, and each of them, pursuant to 35 U.S.C. § 271.

74. Toshiba America has infringed and continues to infringe the patents-in-suit, and each of them, by its manufacture, use, sale, importation, and/or offer for sale of infringing products including Toshiba microprocessors and microcontrollers and products embodying Toshiba microprocessors and microcontrollers; and its contributing to and inducement of others to manufacture, use, sell, import, and/or offer for sale infringing products. Toshiba America is liable for its infringement of the patents-in-suit, and each of them, pursuant to 35 U.S.C. § 271.

75. Toshiba Electronic has infringed and continues to infringe the patents-in-suit, and each of them, by its manufacture, use, sale, importation, and/or offer for sale of infringing products including Toshiba microprocessors and microcontrollers and products embodying Toshiba microprocessors and microcontrollers; and its contributing to and inducement of others to manufacture, use, sell, import, and/or offer for sale infringing products. Toshiba Electronic is liable for its infringement of the patents-in-suit, and each of them, pursuant to 35 U.S.C. § 271.

76. Toshiba Information has infringed and continues to infringe the patents-in-suit, and each of them, by its manufacture, use, sale, importation, and/or offer for sale of infringing products including Toshiba microprocessors and microcontrollers and products embodying Toshiba microprocessors and microcontrollers; and its contributing to and inducement of others to manufacture, use, sell, import, and/or offer for sale infringing products. Toshiba Information is liable for its infringement of the patents-in-suit, and each of them, pursuant to 35 U.S.C. § 271.

77. Toshiba Consumer has infringed and continues to infringe the patents-in-suit, and each of them, by its manufacture, use, sale, importation, and/or offer for sale of infringing products including Toshiba microprocessors and microcontrollers and products embodying

Toshiba microprocessors and microcontrollers; and its contributing to and inducement of others to manufacture, use, sell, import, and/or offer for sale infringing products. Toshiba Consumer is liable for its infringement of the patents-in-suit, and each of them, pursuant to 35 U.S.C. § 271.

78. Toshiba's acts of infringement have caused damage to plaintiff and plaintiff is entitled to recover from Toshiba the damages sustained by it as a result of Toshiba's wrongful acts in an amount subject to proof at trial. Toshiba's infringement of plaintiff's rights under the patents-in-suit will continue to damage plaintiff, causing irreparable harm for which there is no adequate remedy at law unless enjoined by this Court.

79. Toshiba America's acts of infringement have caused damage to plaintiff and plaintiff is entitled to recover from Toshiba America the damages sustained by it as a result of Toshiba America's wrongful acts in an amount subject to proof at trial. Toshiba America's infringement of plaintiff's rights under the patents-in-suit will continue to damage plaintiff, causing irreparable harm for which there is no adequate remedy at law unless enjoined by this Court.

80. Toshiba Electronic's acts of infringement have caused damage to plaintiff and plaintiff is entitled to recover from Toshiba Electronic the damages sustained by it as a result of Toshiba Electronic's wrongful acts in an amount subject to proof at trial. Toshiba Electronic's infringement of plaintiff's rights under the patents-in-suit will continue to damage plaintiff, causing irreparable harm for which there is no adequate remedy at law unless enjoined by this Court.

81. Toshiba Information's acts of infringement have caused damage to plaintiff and plaintiff is entitled to recover from Toshiba Information the damages sustained by it as a result of Toshiba Information's wrongful acts in an amount subject to proof at trial. Toshiba Information's infringement of plaintiff's rights under the patents-in-suit will continue to damage plaintiff, causing irreparable harm for which there is no adequate remedy at law unless enjoined by this Court.

82. Toshiba Consumer's acts of infringement have caused damage to plaintiff and plaintiff is entitled to recover from Toshiba Consumer the damages sustained by it as a result of

Toshiba's wrongful acts in an amount subject to proof at trial. Toshiba Consumer's infringement of plaintiff's rights under the patents-in-suit will continue to damage plaintiff, causing irreparable harm for which there is no adequate remedy at law unless enjoined by this Court.

83. Upon information and belief, Toshiba's infringement of the patents-in-suit is willful and deliberate, entitling plaintiff to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

84. Upon information and belief, Toshiba America's infringement of the patents-in-suit is willful and deliberate, entitling plaintiff to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

85. Upon information and belief, Toshiba Electronic's infringement of the patents-in-suit is willful and deliberate, entitling plaintiff to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

86. Upon information and belief, Toshiba Information's infringement of the patents-in-suit is willful and deliberate, entitling plaintiff to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

87. Upon information and belief, Toshiba Consumer's infringement of the patents-in-suit is willful and deliberate, entitling plaintiff to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

PRAYER FOR RELIEF

WHEREFORE, plaintiff requests entry of judgment in its favor and against defendants, and each of them, as follows:

- a) An award of damages adequate to compensate plaintiff for the infringement alleged herein, together with prejudgment interest thereon;
- b) Enhanced damages pursuant to 35 U.S.C. § 284;
- c) An award of attorneys' fees pursuant to 35 U.S.C. § 285 or as otherwise permitted by law;

d) A permanent injunction prohibiting defendants and their respective officers, agents, employees and those acting in privity with them, from further infringement of the patents-in-suit;

e) Costs of suit; and

f) For such other and further relief as the Court may deem just and proper.

DATED: October 24, 2005

Respectfully submitted,

By:

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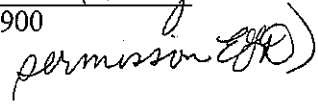
TECHNOLOGY PROPERTIES LIMITED, INC

DEMAND FOR JURY TRIAL

Plaintiff TPL hereby demands trial by jury of all issues so triable in this matter.

DATED: October 24, 2005

Respectfully submitted,

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EXHIBIT A



US006598148B1

(12) **United States Patent**
Moore et al.

(10) Patent No.: **US 6,598,148 B1**
(45) Date of Patent: **Jul. 22, 2003**

(54) **HIGH PERFORMANCE MICROPROCESSOR
HAVING VARIABLE SPEED SYSTEM
CLOCK**

(56) **References Cited**

U.S. PATENT DOCUMENTS

(75) Inventors: Charles H. Moore, Woodside, CA
(US); Russell H. Fish, III, Dallas, TX
(US)

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* cited by examiner

(73) Assignee: Patriot Scientific Corporation, Poway,
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(*) Notice: Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 0 days

Primary Examiner—David Y. Eng
(74) Attorney, Agent, or Firm—Knobbe Martens Olson &
Bear LLP

(57) ABSTRACT

A microprocessor integrated circuit including a processing unit disposed upon an integrated circuit substrate is disclosed herein. The processing unit is designed to operate in accordance with a predefined sequence of program instructions stored within an instruction register. A memory, capable of storing information provided by the processing unit and occupying a larger area of the integrated circuit substrate than the processing unit, is also provided within the microprocessor integrated circuit. The memory may be implemented using, for example dynamic or static random-access memory. A variable output frequency system clock, such as generated by a ring oscillator, is also disposed on the integrated circuit substrate.

(21) Appl No.: 09/124,623

(22) Filed: Jul 29, 1998

(Under 37 CFR 1.47)

Related U.S. Application Data

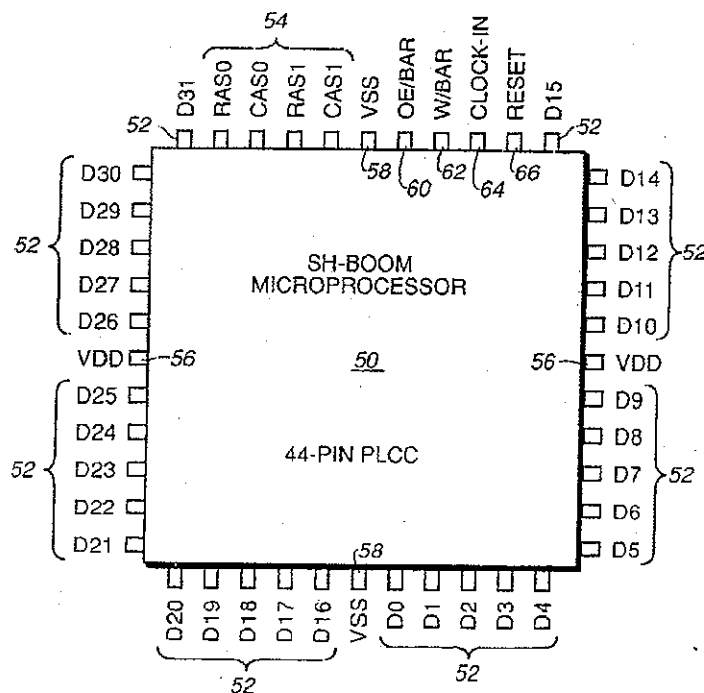
(62) Division of application No. 08/484,918, filed on Jun 7, 1995, now Pat. No. 5,809,336, which is a division of application No. 07/389,334, filed on Aug 3, 1989, now Pat. No. 5,440,749

(51) Int. Cl.⁷ G06F 15/00

(52) U.S. Cl. 712/32

(58) Field of Search 712/32; 711/104,
711/105

13 Claims, 19 Drawing Sheets



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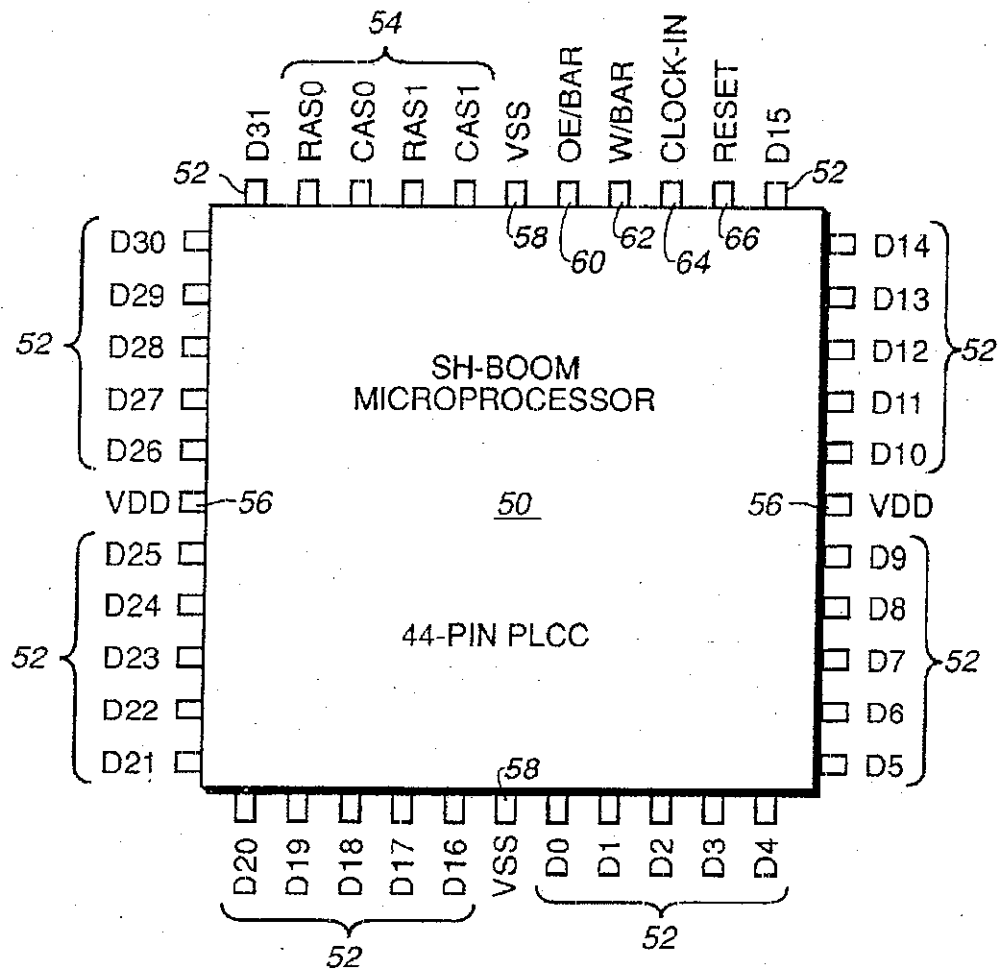


FIG. 1

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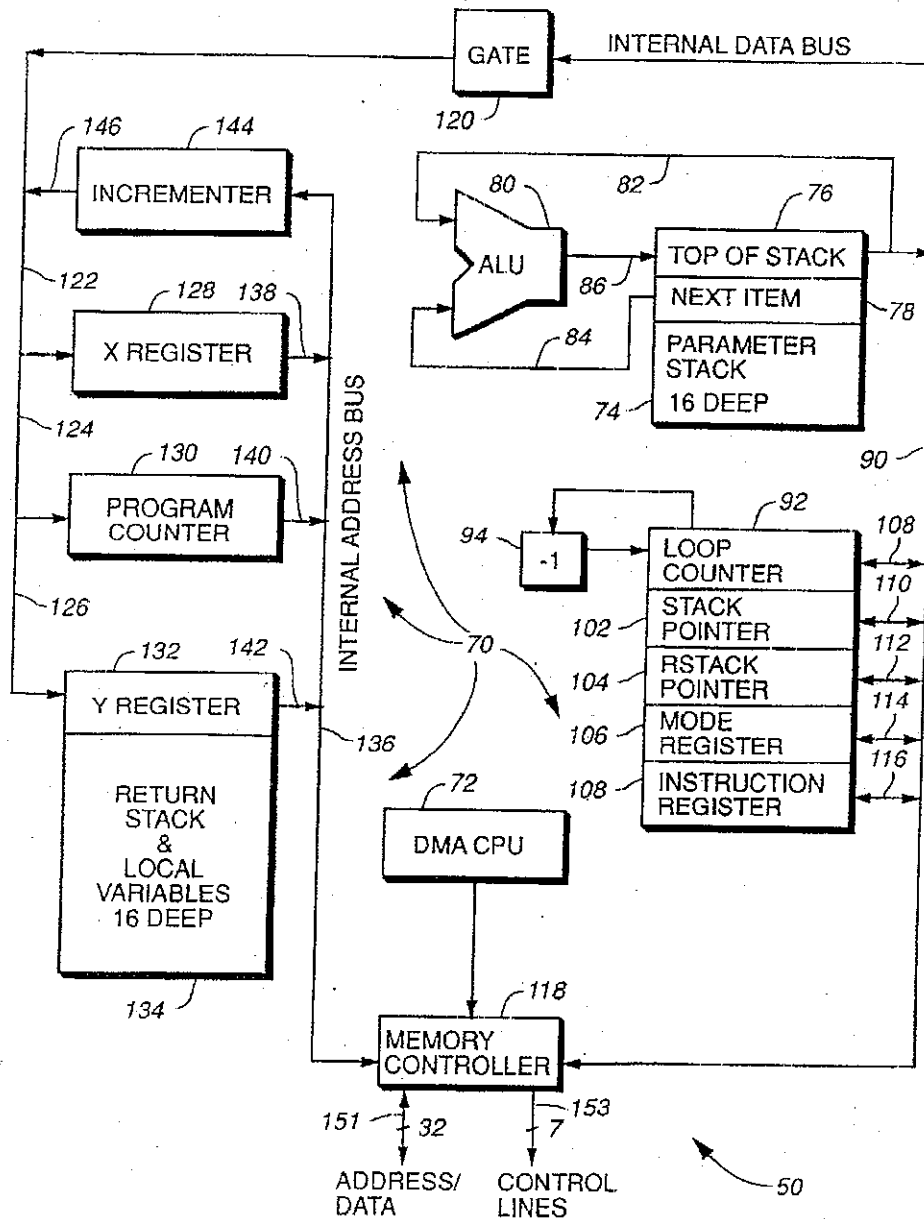


FIG. 2

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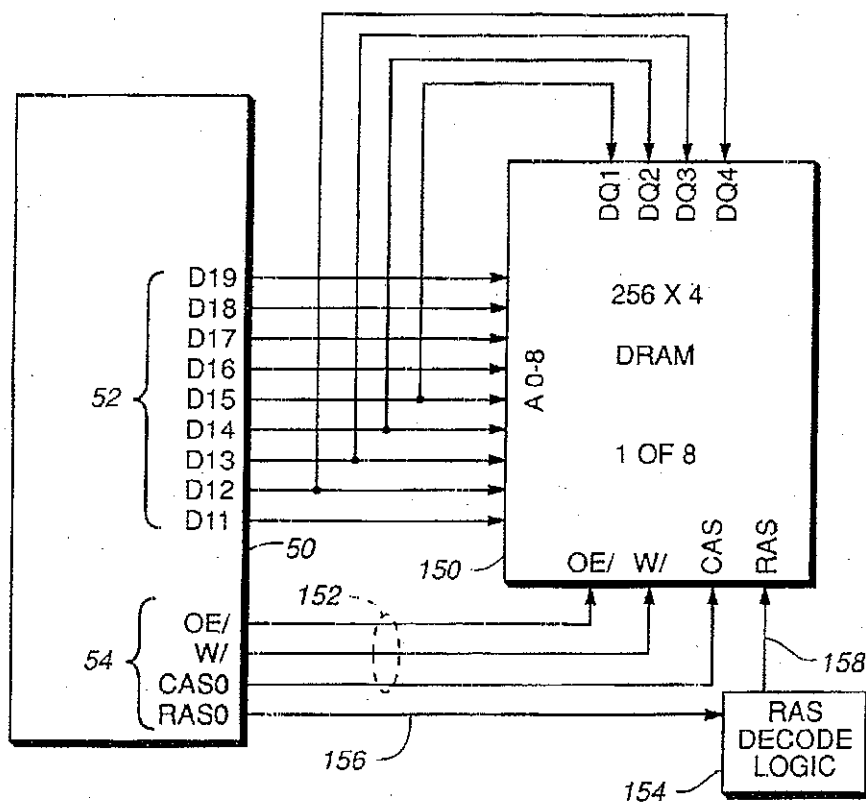


FIG. 3

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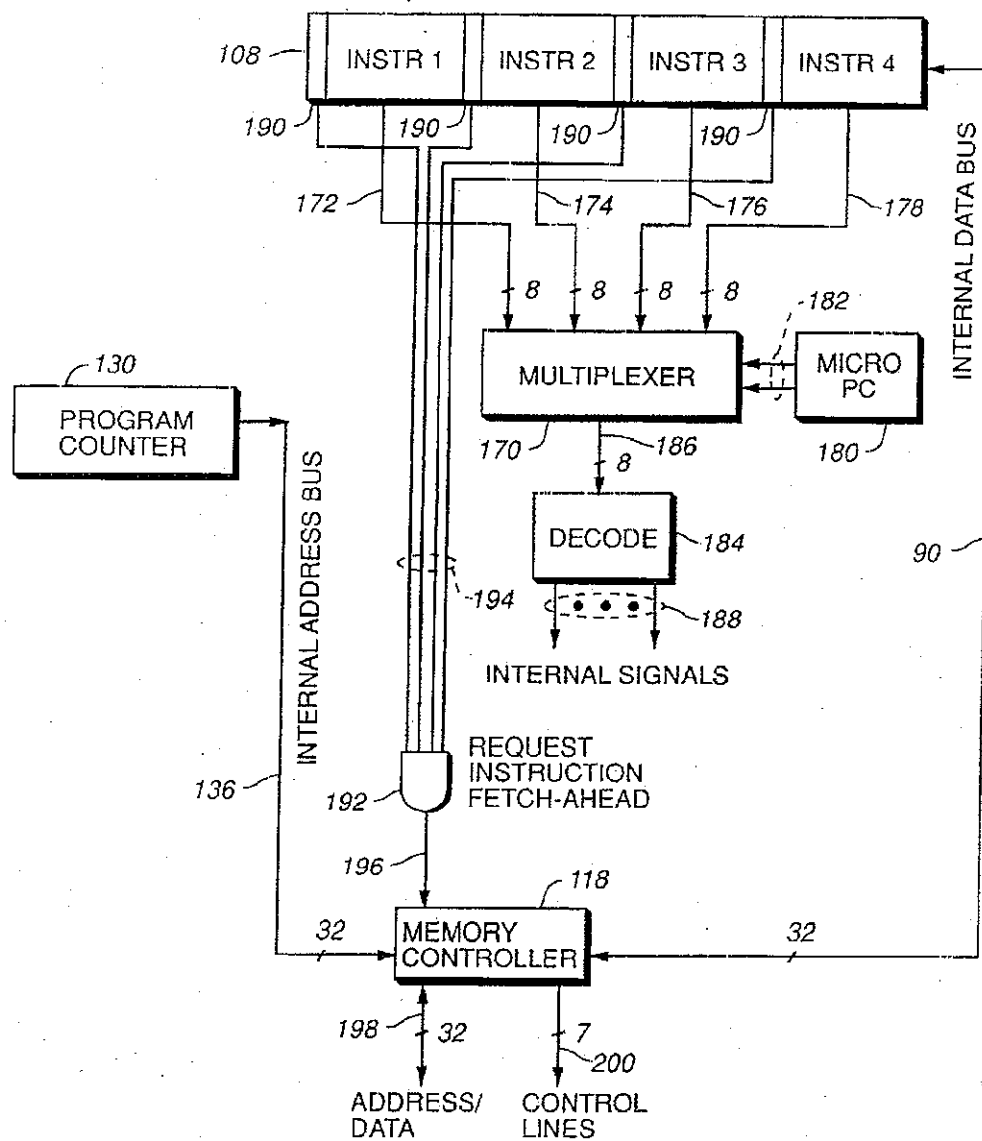


FIG. 4

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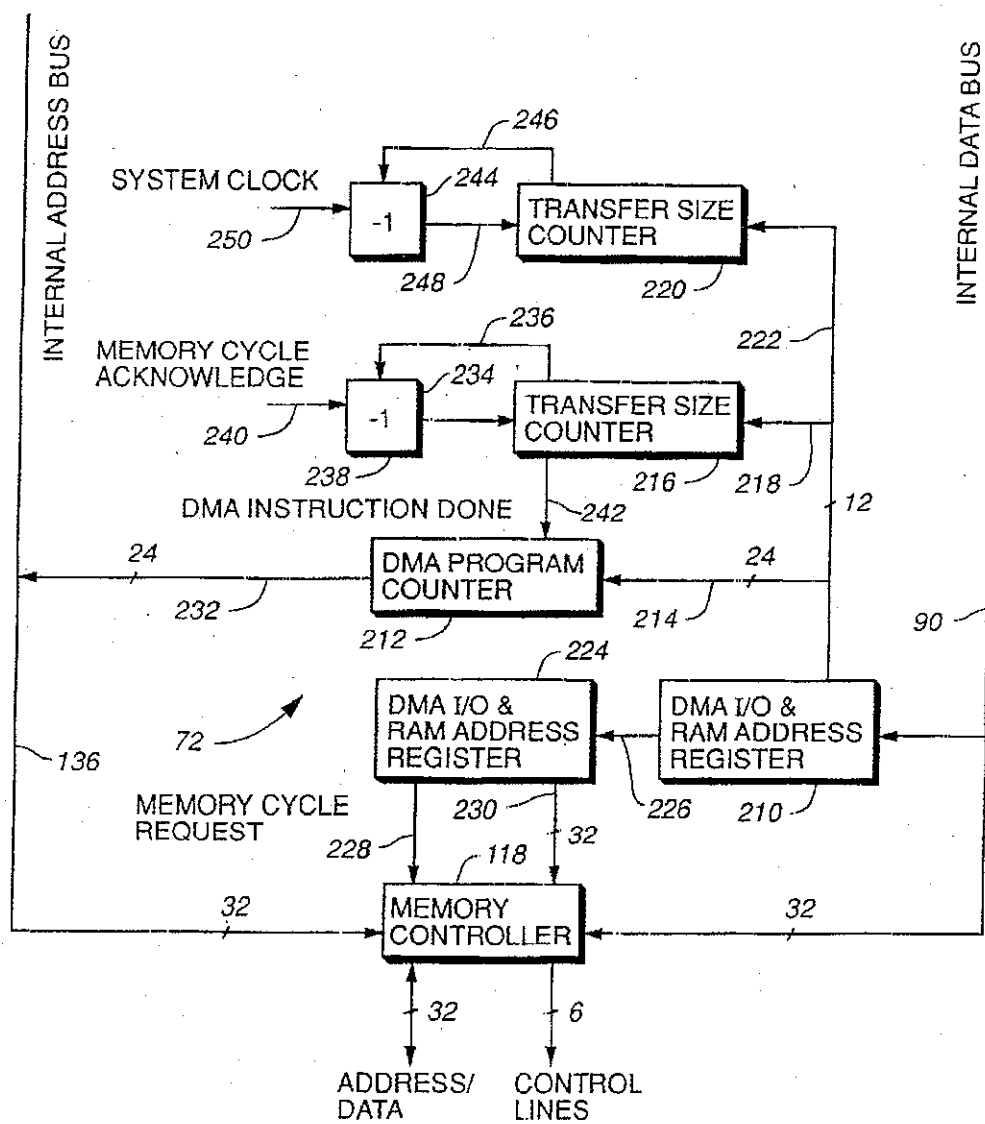


FIG. 5

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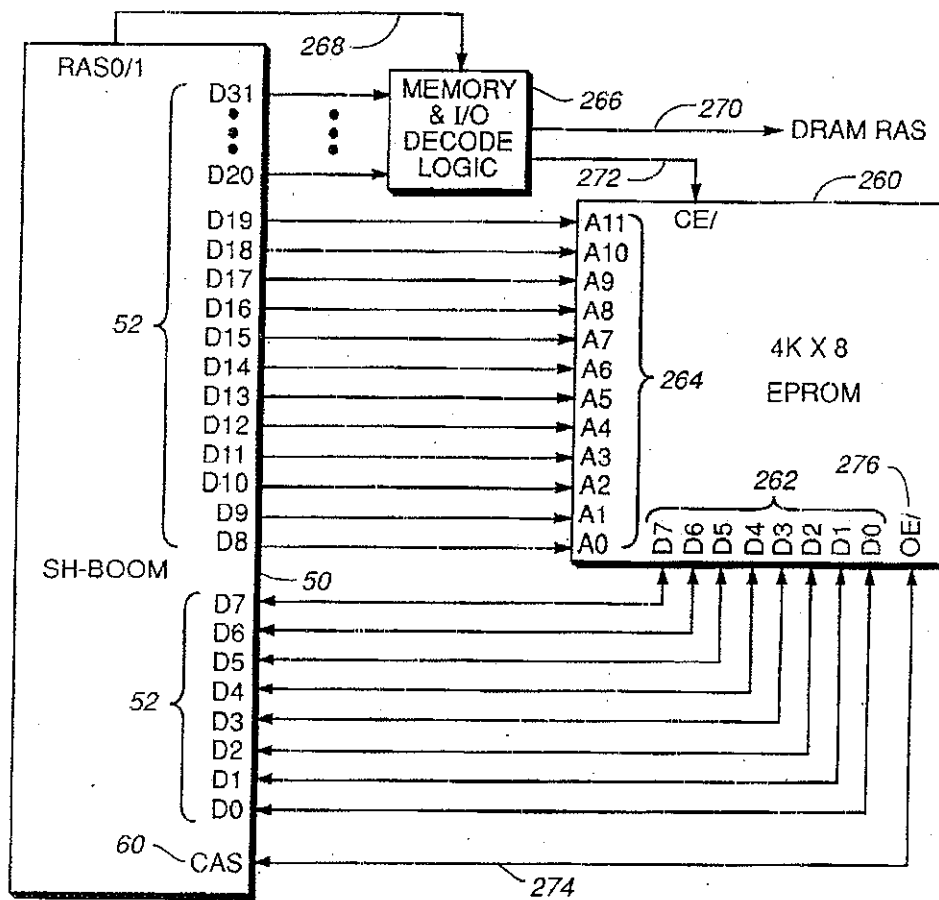


FIG. 6

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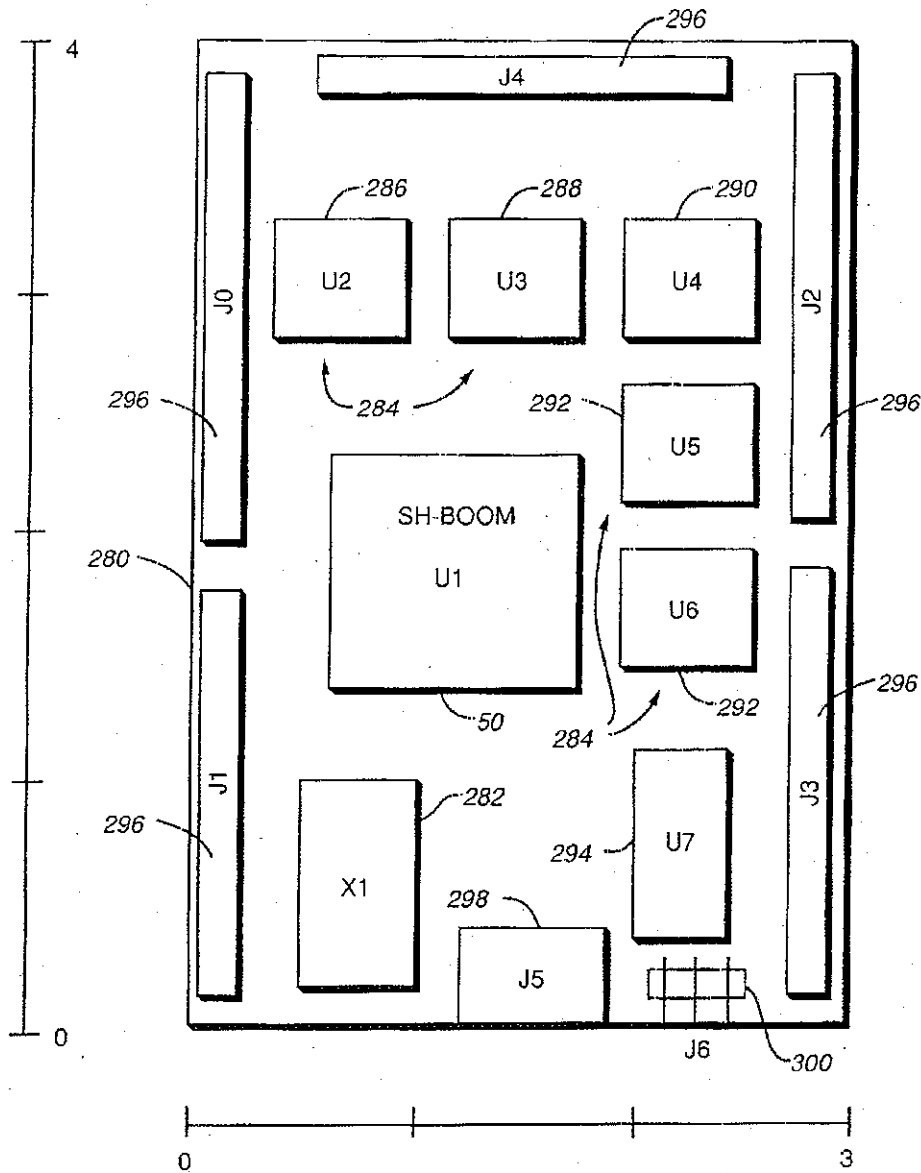


FIG. 7

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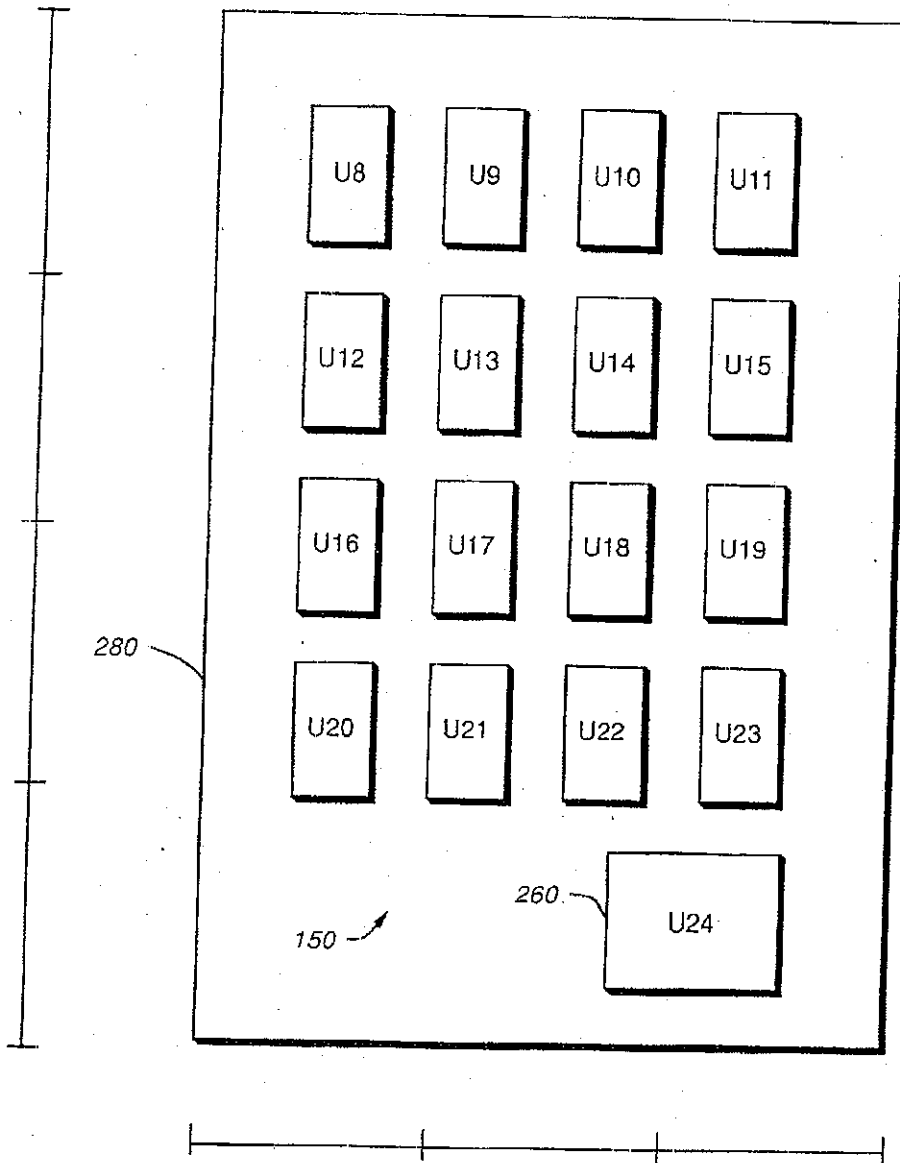


FIG. 8

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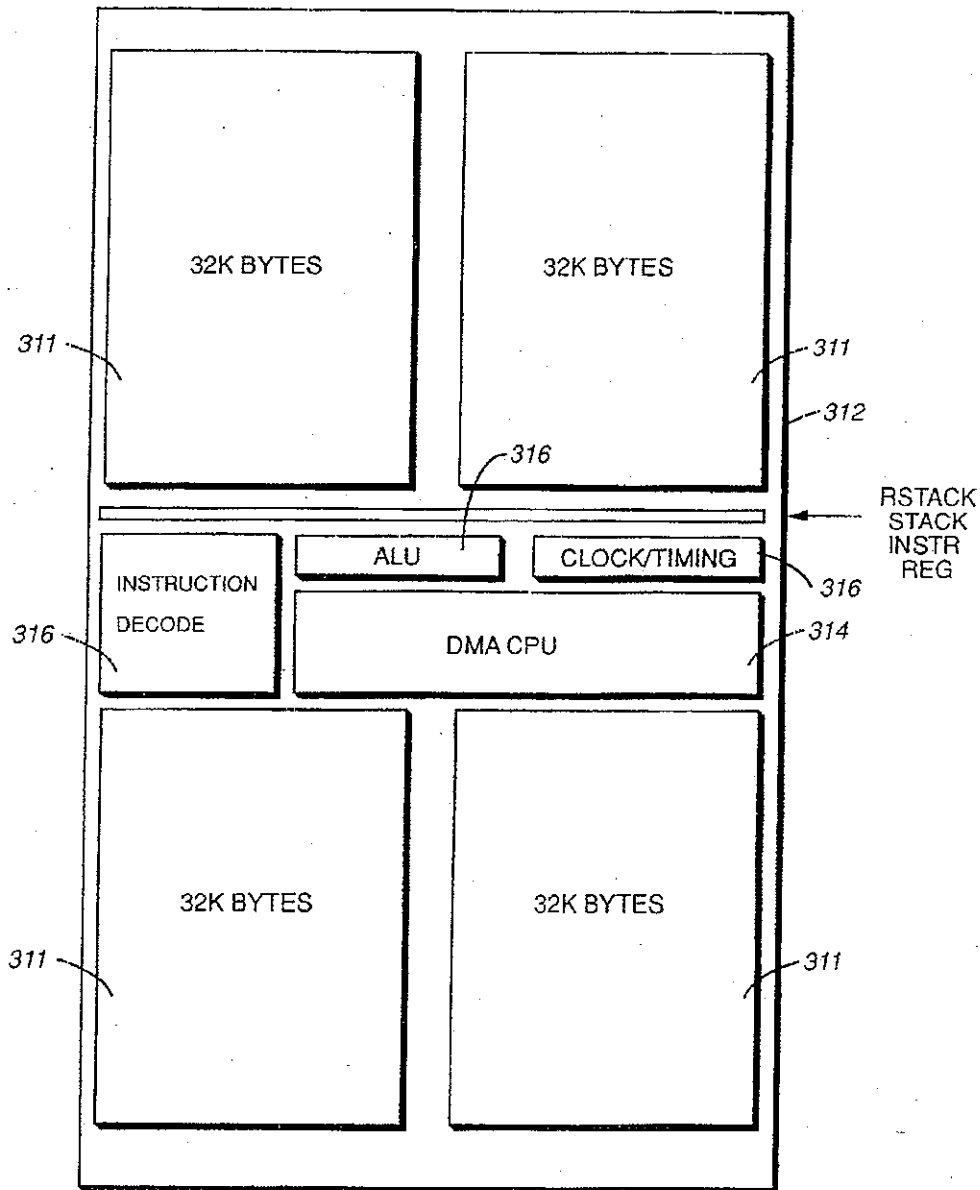


FIG. 9

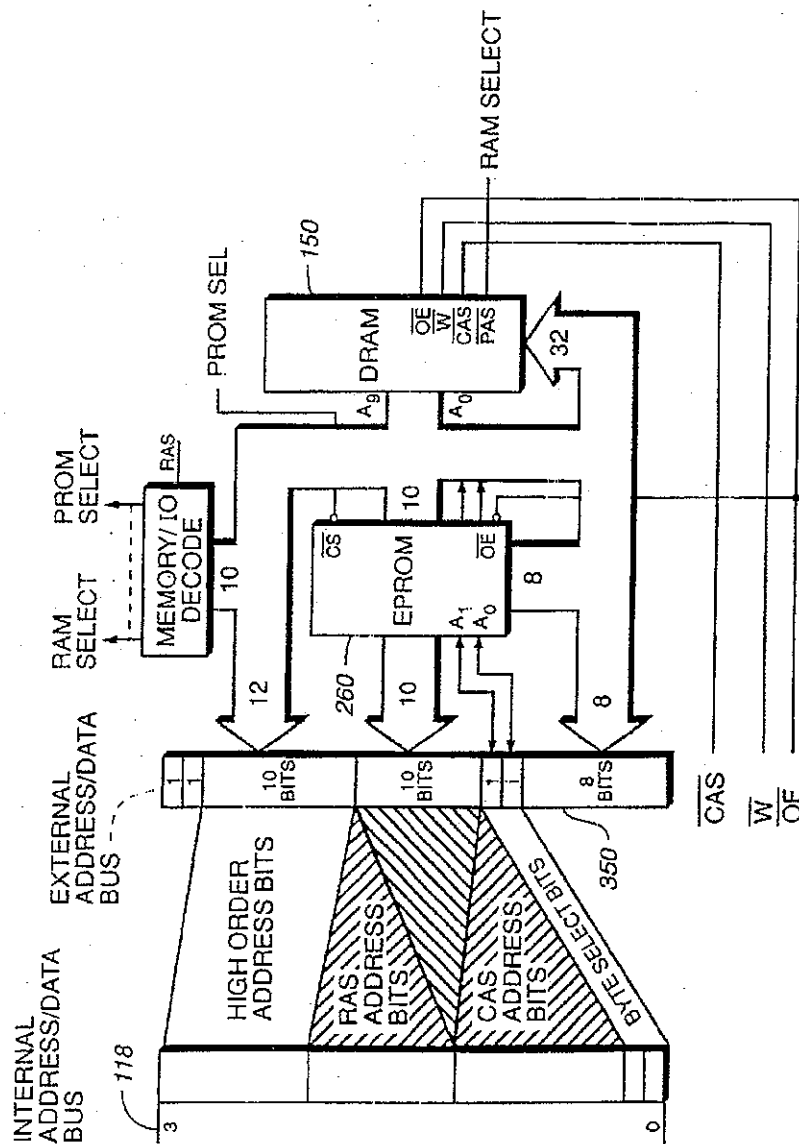


FIG. 10

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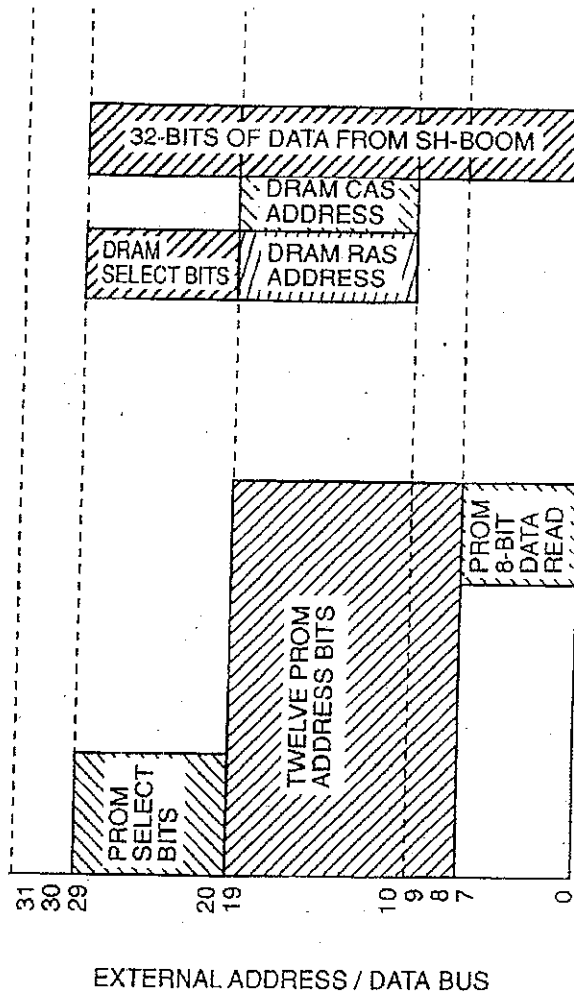
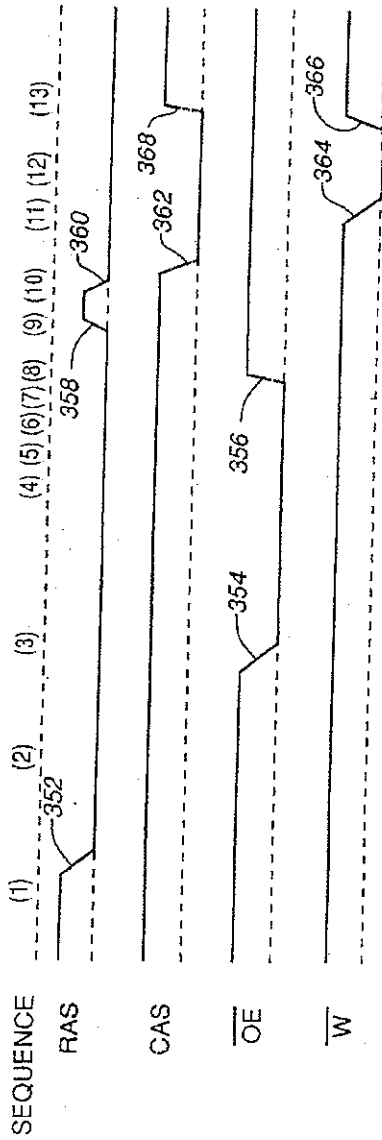


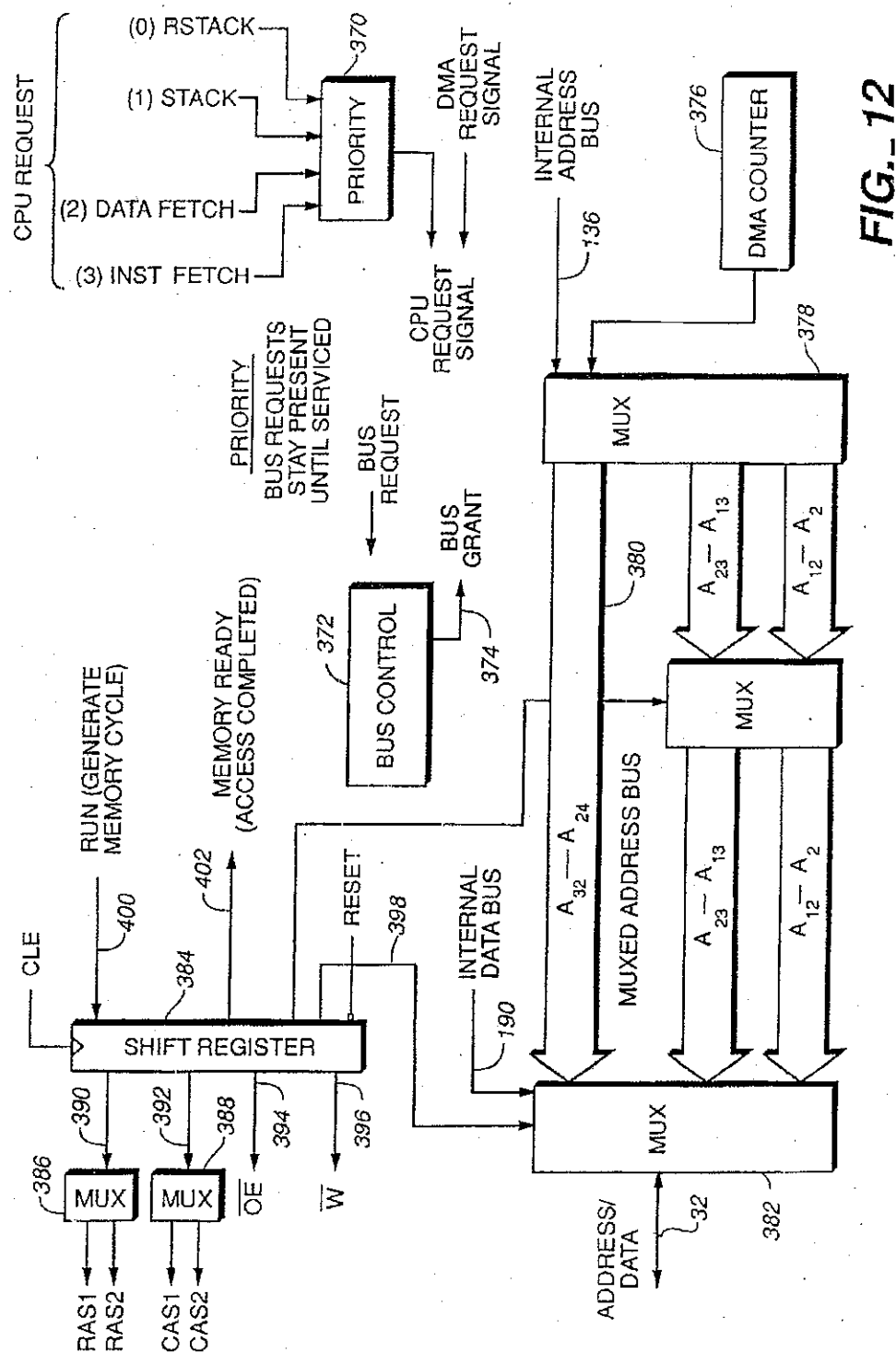
FIG. 11

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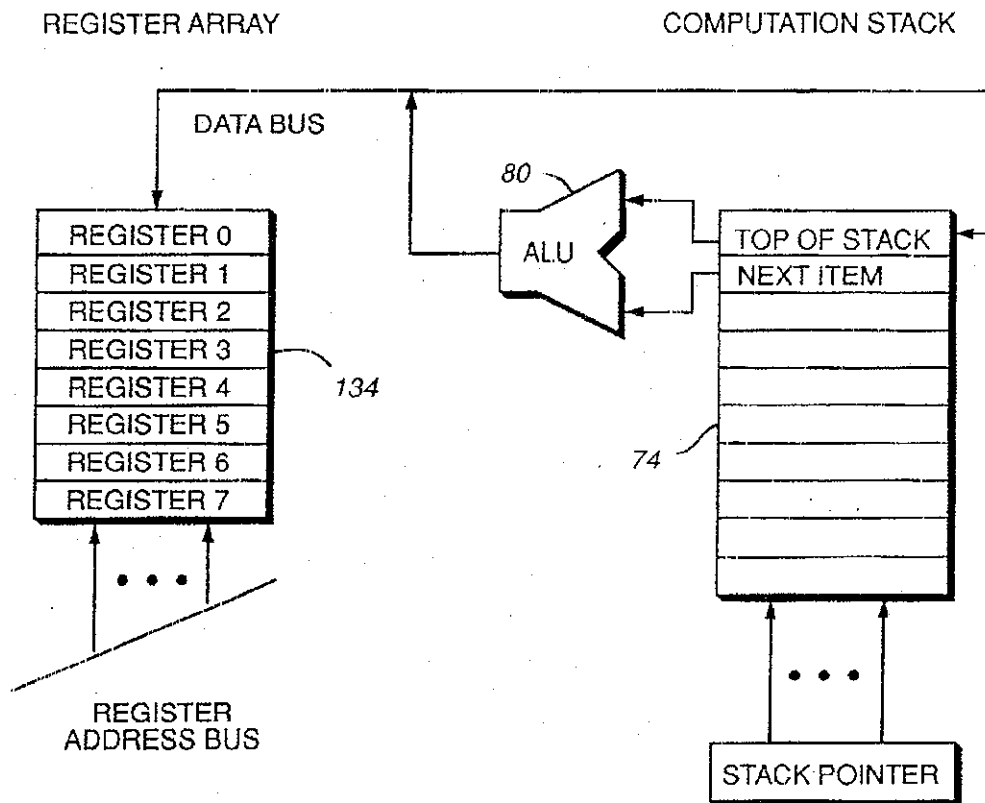


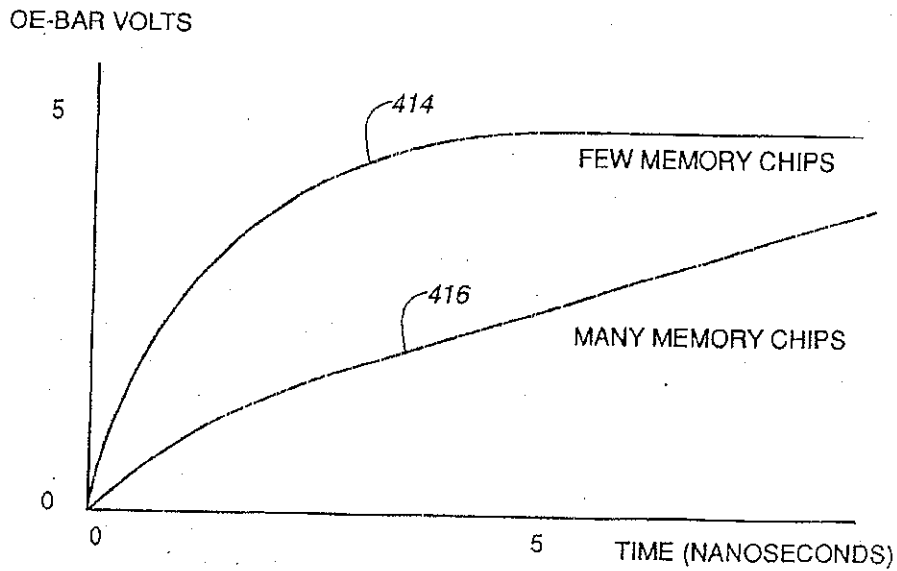
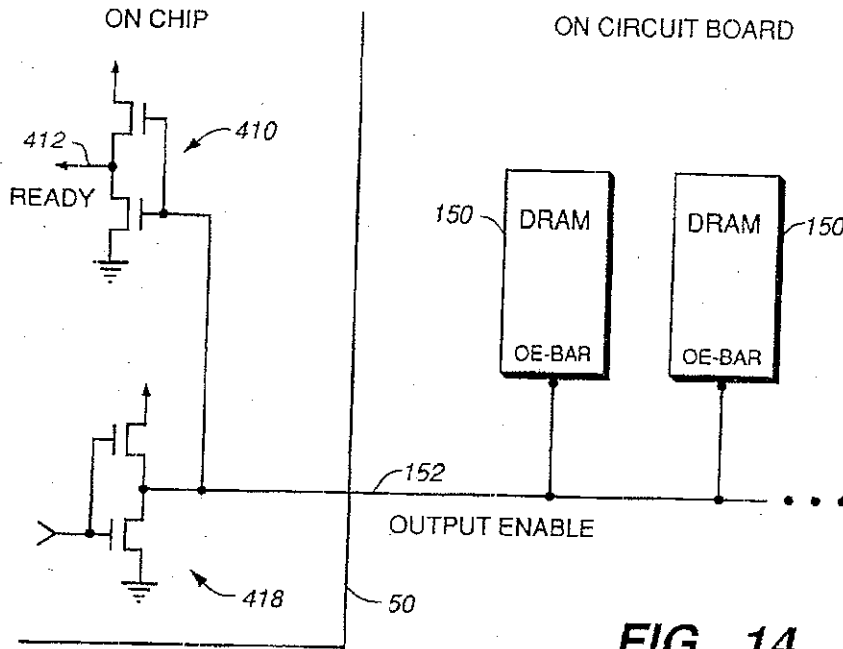
FIG. 13

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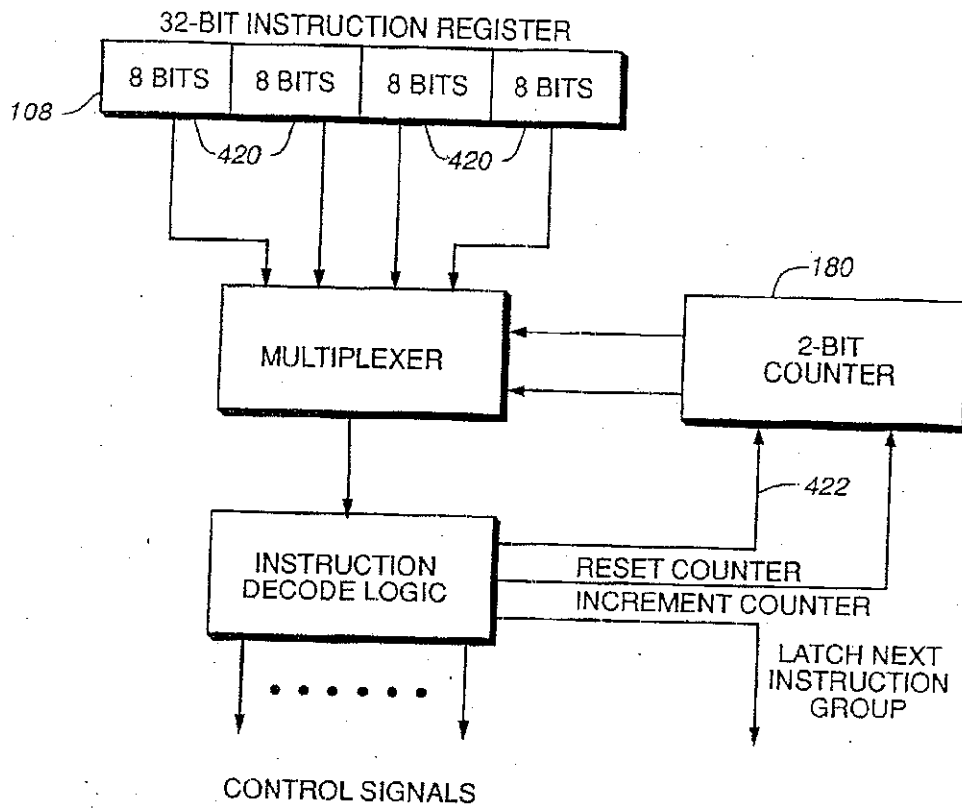
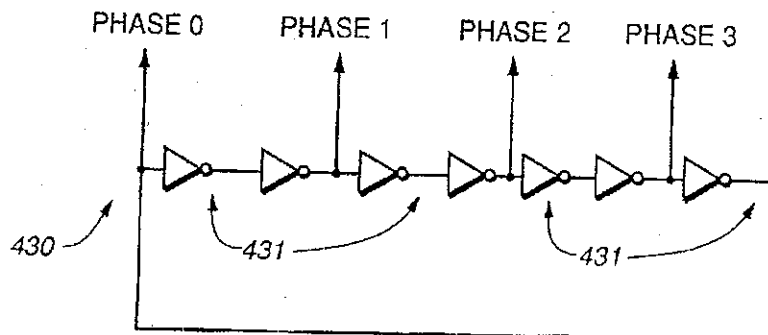


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**FIG. 16****FIG. 18**

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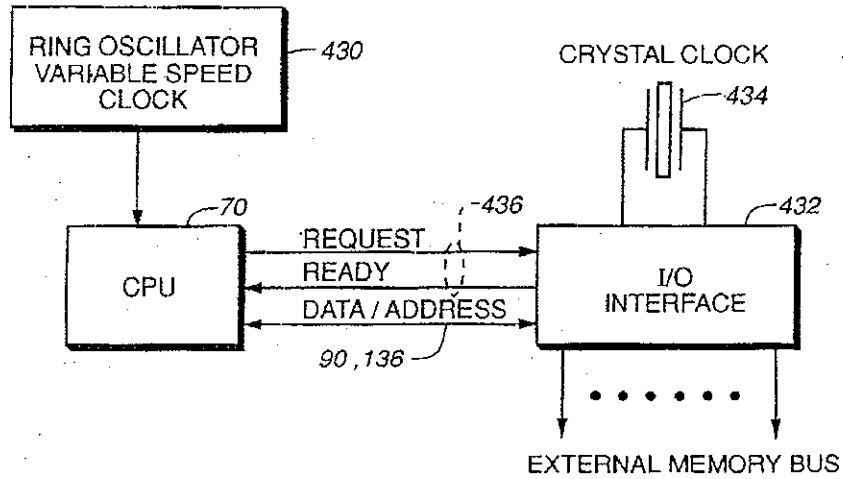


FIG. 17

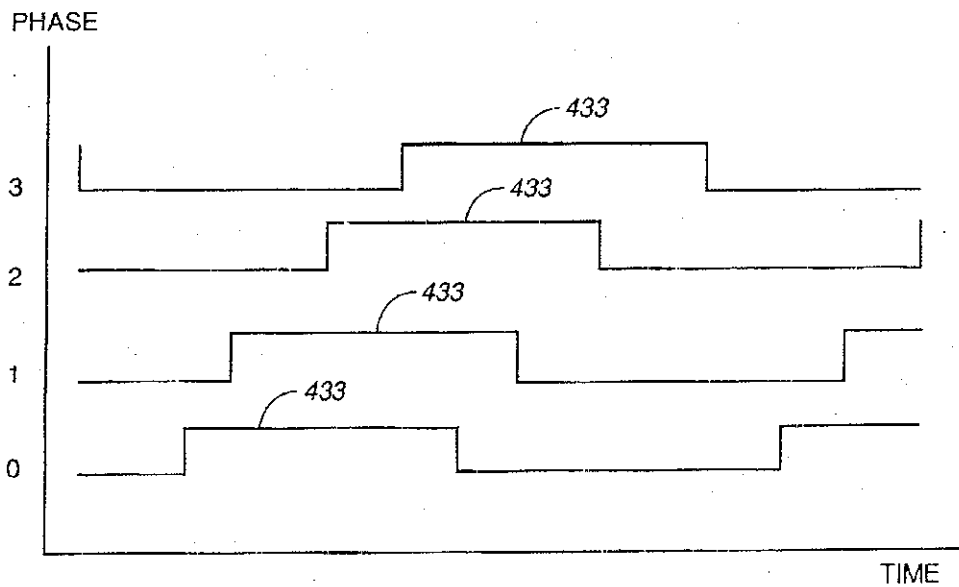


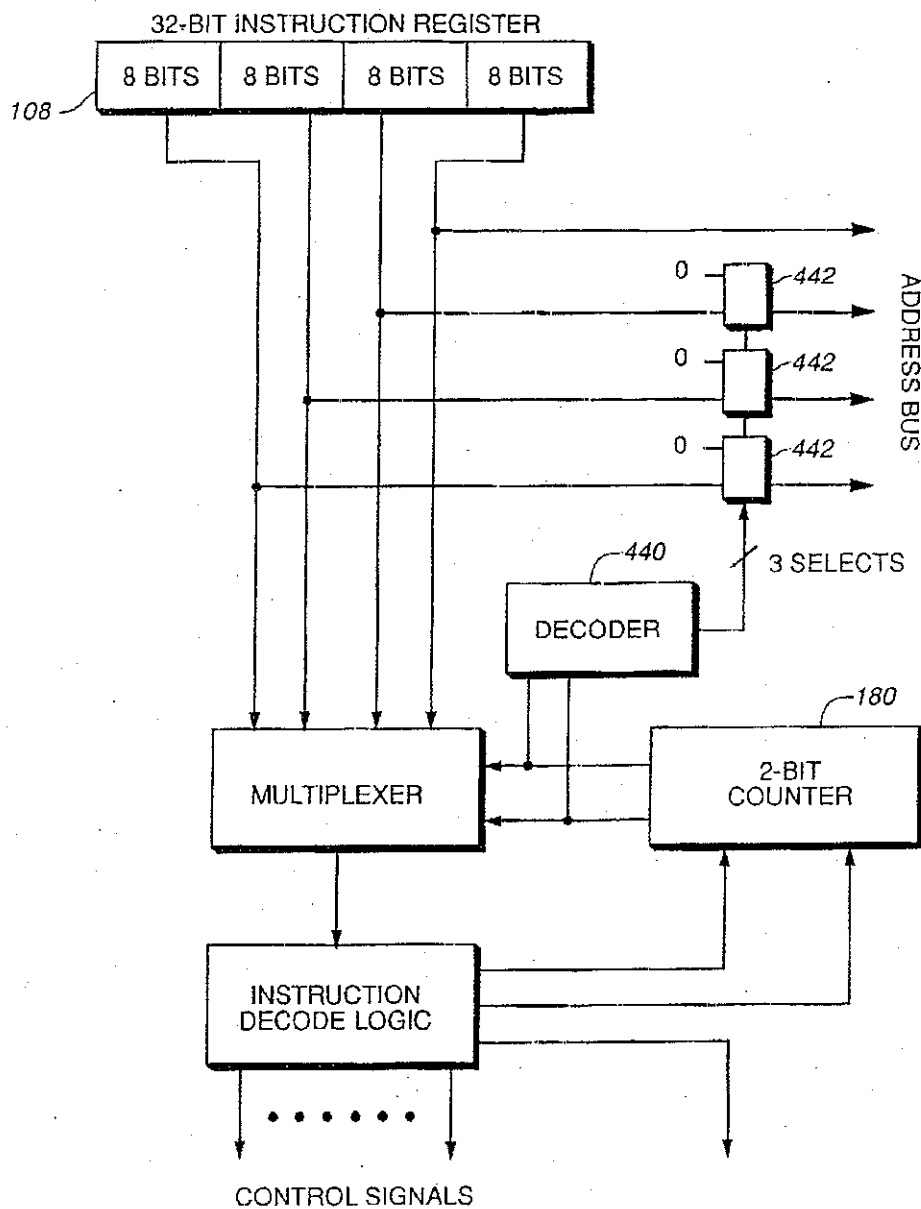
FIG. 19

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**FIG. 20**

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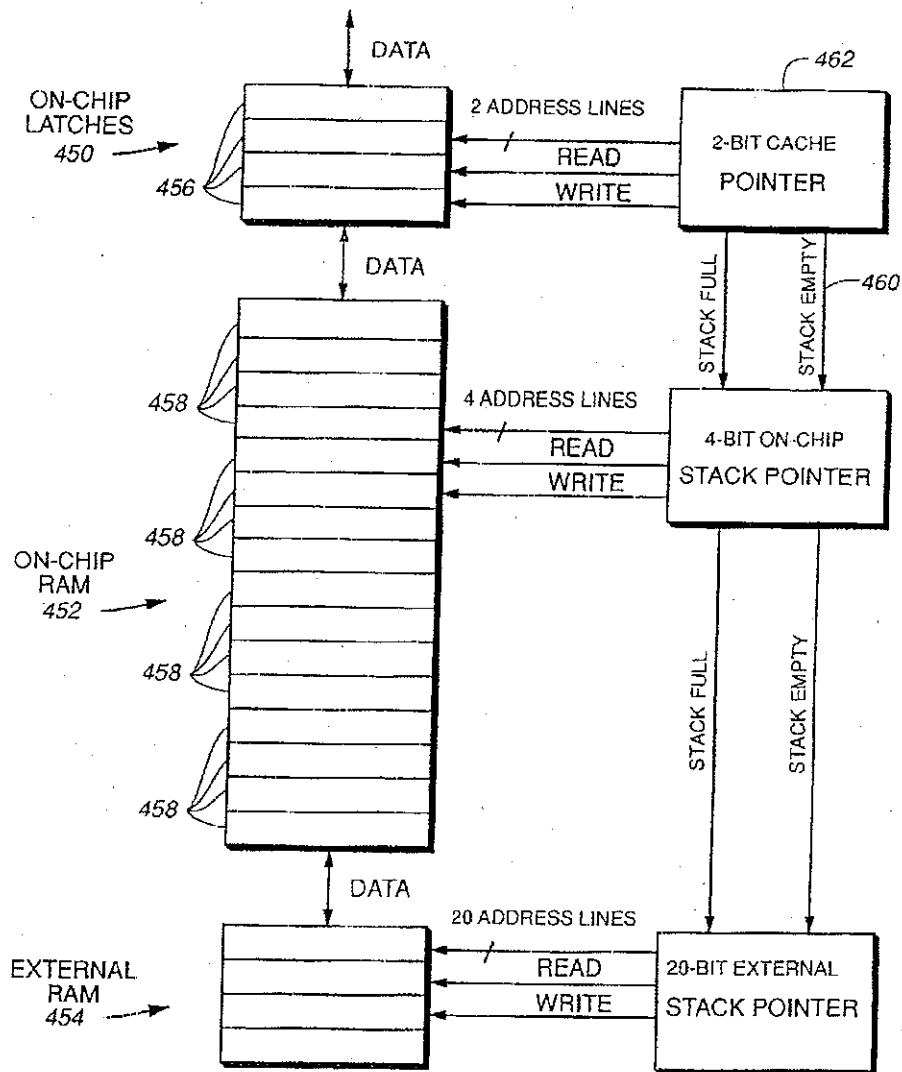


FIG. 21

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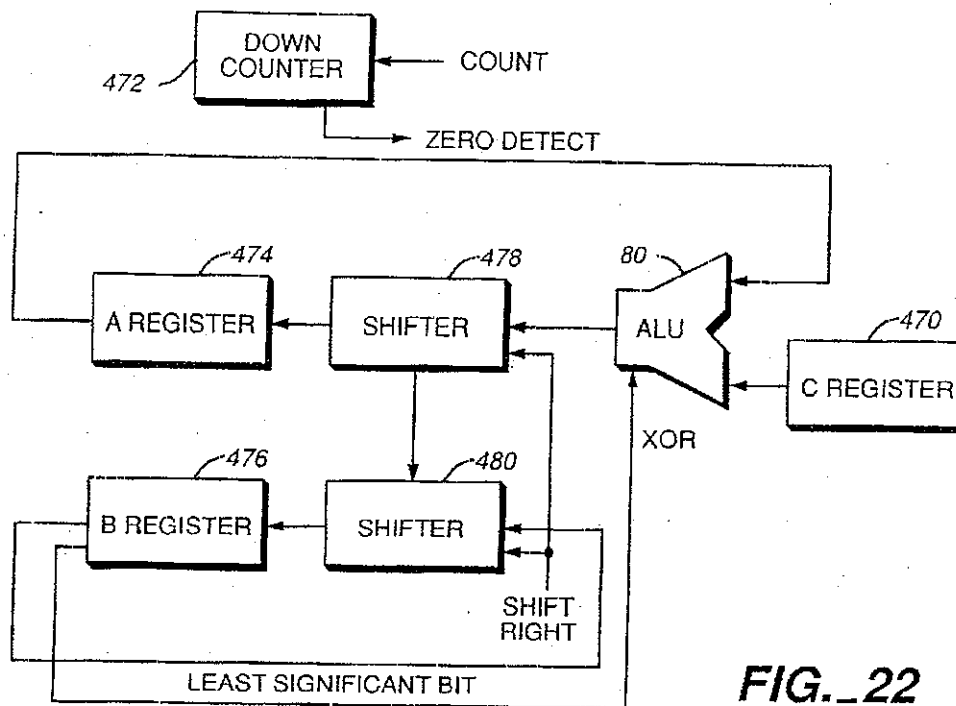


FIG. 22

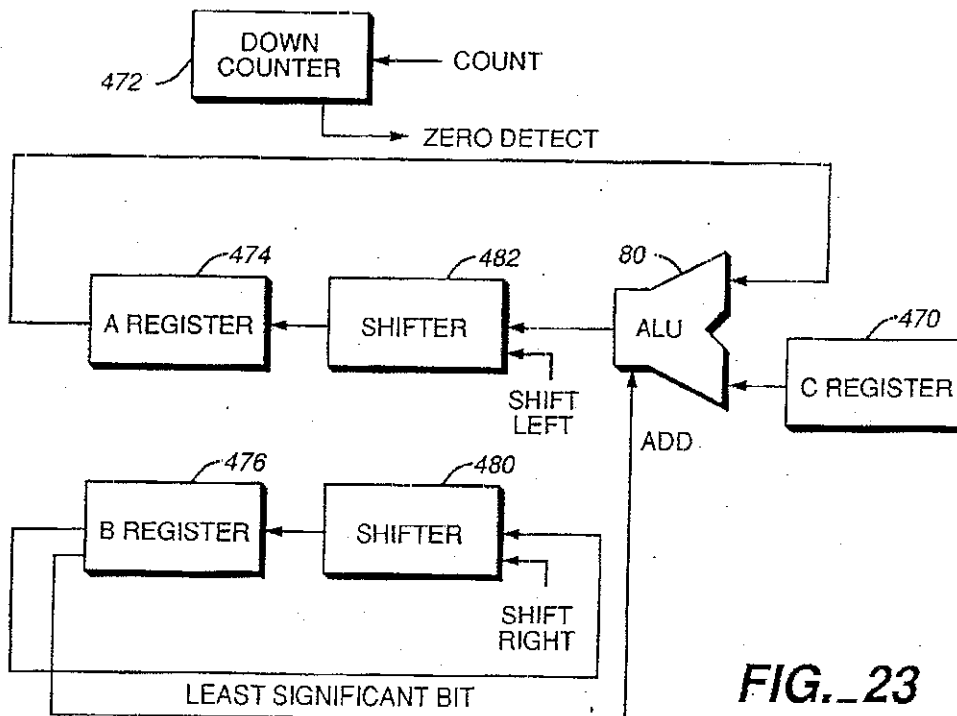


FIG. 23

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HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK

This application is a divisional of U.S. patent application No. 08/484,918, filed Jun. 7, 1995, now U.S. Pat. No. 5,809,336 which is a divisional of U.S. patent application No. 07/389,334, filed Aug. 3, 1989 now U.S. Pat. No. 5,982,231.

BACKGROUND OF THE INVENTION

1 Field of the Invention

The present invention relates generally to a simplified, reduced instruction set computer (RISC) microprocessor. More particularly, it relates to such a microprocessor which is capable of performance levels of, for example, 20 million instructions per second (MIPS) at a price of, for example, 20 dollars.

2 Description of the Prior Art

Since the invention of the microprocessor, improvements in its design have taken two different approaches. In the first approach, a brute force gain in performance has been achieved through the provision of greater numbers of faster transistors in the microprocessor integrated circuit and an instruction set of increased complexity. This approach is exemplified by the Motorola 68000 and Intel 80X86 microprocessor families. The trend in this approach is to larger die sizes and packages, with hundreds of pinouts.

More recently, it has been perceived that performance gains can be achieved through comparative simplicity, both in the microprocessor integrated circuit itself and in its instruction set. This second approach provides RISC microprocessors, and is exemplified by the Sun SPARC and the Intel 8960 microprocessors. However, even with this approach as conventionally practiced, the packages for the microprocessor are large, in order to accommodate the large number of pinouts that continue to be employed. A need therefore remains for further simplification of high performance microprocessors.

With conventional high performance microprocessors, fast static memories are required for direct connection to the microprocessors in order to allow memory accesses that are fast enough to keep up with the microprocessors. Slower dynamic random access memories (DRAMs) are used with such microprocessors only in a hierarchical memory arrangement, with the static memories acting as a buffer between the microprocessors and the DRAMs. The necessity to use static memories increases cost of the resulting systems.

Conventional microprocessors provide direct memory accesses (DMA) for system peripheral units through DMA controllers, which may be located on the microprocessor integrated circuit, or provided separately. Such DMA controllers can provide routine handling of DMA requests and responses, but some processing by the main central processing unit (CPU) of the microprocessor is required.

SUMMARY OF THE INVENTION

Accordingly, it is an object of this invention to provide a microprocessor with a reduced pin count and cost compared to conventional microprocessors.

It is another object of the invention to provide a high performance microprocessor that can be directly connected to DRAMs without sacrificing microprocessor speed.

It is a further object of the invention to provide a high performance microprocessor in which DMA does not

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require use of the main CPU during DMA requests and responses and which provides very rapid DMA response with predictable response times.

The attainment of these and related objects may be achieved through use of the novel high performance, low cost microprocessor herein disclosed. The microprocessor integrated circuit includes a processing unit disposed upon an integrated circuit substrate. In a preferred implementation the processing unit operates in accordance with a predefined sequence of program instructions stored within an instruction register. A memory, capable of storing information provided by the processing unit and occupying a larger area of the integrated circuit substrate than the processing unit, is also provided within the microprocessor integrated circuit. The memory may be implemented using, for example, dynamic or static random-access memory.

The attainment of the foregoing and related objects, advantages and features of the invention should be more readily apparent to those skilled in the art, after review of the following more detailed description of the invention, taken together with the drawings, in which:

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is an external, plan view of an integrated circuit package incorporating a microprocessor in accordance with the invention.

FIG. 2 is a block diagram of a microprocessor in accordance with the invention.

FIG. 3 is a block diagram of a portion of a data processing system incorporating the microprocessor of FIGS. 1 and 2.

FIG. 4 is a more detailed block diagram of a portion of the microprocessor shown in FIG. 2.

FIG. 5 is a more detailed block diagram of another portion of the microprocessor shown in FIG. 2.

FIG. 6 is a block diagram of another portion of the data processing system shown in part in FIG. 3 and incorporating the microprocessor of FIGS. 1-2 and 4-5.

FIGS. 7 and 8 are layout diagrams for the data processing system shown in part in FIGS. 3 and 6.

FIG. 9 is a layout diagram of a second embodiment of a microprocessor in accordance with the invention in a data processing system on a single integrated circuit.

FIG. 10 is a more detailed block diagram of a portion of the data processing system of FIGS. 7 and 8.

FIG. 11 is a timing diagram useful for understanding operation of the system portion shown in FIG. 12.

FIG. 12 is another more detailed block diagram of a further portion of the data processing system of FIGS. 7 and 8.

FIG. 13 is a more detailed block diagram of a portion of the microprocessor shown in FIG. 2.

FIG. 14 is a more detailed block and schematic diagram of a portion of the system shown in FIGS. 3 and 7-8.

FIG. 15 is a graph useful for understanding operation of the system portion shown in FIG. 14.

FIG. 16 is a more detailed block diagram showing part of the system portion shown in FIG. 4.

FIG. 17 is a more detailed block diagram of a portion of the microprocessor shown in FIG. 2.

FIG. 18 is a more detailed block diagram of part of the microprocessor portion shown in FIG. 17.

FIG. 19 is a set of waveform diagrams useful for understanding operation of the part of the microprocessor portion shown in FIG. 18.

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FIG 20 is a more detailed block diagram showing another part of the system portion shown in FIG 4.

FIG 21 is a more detailed block diagram showing another part of the system portion shown in FIG 4.

FIGS 22 and 23 are more detailed block diagrams showing another part of the system portion shown in FIG 4.

DETAILED DESCRIPTION OF THE INVENTION

OVERVIEW

The microprocessor of this invention is desirably implemented as a 32-bit microprocessor optimized for:

HIGH EXECUTION SPEED, and

LOW SYSTEM COST

In this embodiment, the microprocessor can be thought of as 20 MIPS for 20 dollars. Important distinguishing features of the microprocessor are:

Uses low-cost commodity DYNAMIC RAMS to run 20 MIPS

4 instruction fetch per memory cycle

On-chip fast page-mode memory management

Runs fast without external cache

Requires few interfacing chips

Crams 32-bit CPU in 44 pin SOJ package

The instruction set is organized so that most operations can be specified with 8-bit instructions. Two positive products of this philosophy are:

Programs are smaller,

Programs can execute much faster

The bottleneck in most computer systems is the memory bus. The bus is used to fetch instructions and fetch and store data. The ability to fetch four instructions in a single memory bus cycle significantly increases the bus availability to handle data.

Turning now to the drawings, more particularly to FIG 1, there is shown a packaged 32-bit microprocessor 50 in a 44-pin plastic leadless chip carrier, shown approximately 100 times its actual size of about 0.8 inch on a side. The fact that the microprocessor 50 is provided as a 44-pin package represents a substantial departure from typical microprocessor packages, which usually have about 200 input/output (I/O) pins. The microprocessor 50 is rated at 20 million instructions per second (MIPS). Address and data lines 52, also labelled D0-D31, are shared for addresses and data without speed penalty as a result of the manner in which the microprocessor 50 operates, as will be explained below.

DYNAMIC RAM

In addition to the low cost 44-pin package, another unusual aspect of the high performance microprocessor 50 is that it operates directly with dynamic random access memories (DRAMs), as shown by row address strobe (RAS) and column address strobe (CAS) I/O pins 54. The other I/O pins for the microprocessor 50 include VDD pins 56, VSS pins 58, output enable pin 60, write pin 62, clock pin 64 and reset pin 66.

All high speed computers require high speed and expensive memory to keep up. The highest speed static RAM memories cost as much as ten times as much as slower dynamic RAMs. This microprocessor has been optimized to use low-cost dynamic RAM in high-speed page-mode. Page-mode dynamic RAMs offer static RAM performance without the cost penalty. For example, low-cost 85 nsec. dynamic RAMs access at 25 nsec when operated in fast page-mode. Integrated fast page-mode control on the microprocessor chip simplifies system interfacing and results in a faster system.

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Details of the microprocessor 50 are shown in FIG 2. The microprocessor 50 includes a main central processing unit (CPU) 70 and a separate direct memory access (DMA) CPU 72 in a single integrated circuit making up the microprocessor 50. The main CPU 70 has a first 16 deep push down stack 74, which has a top item register 76 and a next item register 78, respectively connected to provide inputs to an arithmetic logic unit (ALU) 80 by lines 82 and 84. An output of the ALU 80 is connected to the top item register 76 by line 86. The output of the top item register at 82 is also connected by line 88 to an internal data bus 90.

A loop counter 92 is connected to a decremter 94 by lines 96 and 98. The loop counter 92 is bidirectionally connected to the internal data bus 90 by line 100. Stack pointer 102, return stack pointer 104, mode register 106 and instruction register 108 are also connected to the internal data bus 90 by lines 110, 112, 114 and 116, respectively. The internal data bus 90 is connected to memory controller 118 and to gate 120. The gate 120 provides inputs on lines 122, 124, and 126 to X register 128, program counter 130 and Y register 132 of return push down stack 134. The X register 128, program counter 130 and Y register 132 provide outputs to internal address bus 136 on lines 138, 140 and 142. The internal address bus provides inputs to the memory controller 118 and to an incrementer 144. The incrementer 144 provides inputs to the X register, program counter and Y register via lines 146, 122, 124 and 126. The DMA CPU 72 provides inputs to the memory controller 118 on line 148. The memory controller 118 is connected to a RAM (not shown) by address/data bus 151 and control lines 153.

FIG 2 shows that the microprocessor 50 has a simple architecture. Prior art RISC microprocessors are substantially more complex in design. For example, the SPARC RISC microprocessor has three times the gates of the microprocessor 50, and the Intel 8960 RISC microprocessor has 20 times the gates of the microprocessor 50. The speed of this microprocessor is in substantial part due to this simplicity. The architecture incorporates push down stacks and register write to achieve this simplicity.

The microprocessor 50 incorporates an I/O that has been tuned to make heavy use of resources provided on the integrated circuit chip. On chip latches allow use of the same I/O circuits to handle three different things: column addressing, row addressing and data, with a slight to non-existent speed penalty. This triple bus multiplexing results in fewer buffers to expand, fewer interconnection lines, fewer I/O pins and fewer internal buffers.

The provision of on-chip DRAM control gives a performance equal to that obtained with the use of static RAMs. As a result, memory is provided at 1/4 the system cost of static RAM used in most RISC systems.

The microprocessor 50 fetches 4 instructions per memory cycle; the instructions are in an 8-bit format, and this is a 32-bit microprocessor. System speed is therefore 4 times the memory bus bandwidth. This ability enables the microprocessor to break the Von Neumann bottleneck of the speed of getting the next instruction. This mode of operation is possible because of the use of a push down stack and register array. The push down stack allows the use of implied addresses, rather than the prior art technique of explicit addresses for two sources and a destination.

Most instructions execute in 20 nanoseconds in the microprocessor 50. The microprocessor can therefore execute instructions at 50 peak MIPS without pipeline delays. This is a function of the small number of gates in the microprocessor 50 and the high degree of parallelism in the architecture of the microprocessor.

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FIG 3 shows how column and row addresses are multiplexed on lines D8-D14 of the microprocessor 50 for addressing DRAM 150 from I/O pins 52. The DRAM 150 is one of eight, but only one DRAM 150 has been shown for clarity. As shown, the lines D11-D18 are respectively connected to row address inputs A0-A8 of the DRAM 150. Additionally, lines D12-D15 are connected to the data inputs DQ1-DQ4 of the DRAM 150. The output enable, write and column address strobe pins 54 are respectively connected to the output enable, write and column address strobe inputs of the DRAM 150 by lines 152. The row address strobe pin 54 is connected through row address strobe decode logic 154 to the row address strobe input of the DRAM 150 by lines 156 and 158.

D0-D7 pins 52 (FIG. 1) are idle when the microprocessor 50 is outputting multiplexed row and column addresses on D11-D18 pins 52. The D0-D7 pins 52 can therefore simultaneously be used for I/O when right justified I/O is desired. Simultaneous addressing and I/O can therefore be carried out.

FIG. 4 shows how the microprocessor 50 is able to achieve performance equal to the use of static RAMS with DRAMs through multiple instruction fetch in a single clock cycle and instruction fetch-ahead. Instruction register 108 receives four 8-bit byte instruction words 1-4 on 32-bit internal data bus 90. The four instruction byte 1-4 locations of the instruction register 108 are connected to multiplexer 170 by busses 172, 174, 176 and 178, respectively. A microprogram counter 180 is connected to the multiplexer 170 by lines 182. The multiplexer 170 is connected to decoder 184 by bus 186. The decoder 184 provides internal signals to the rest of the microprocessor 50 on lines 188.

Most significant bits 190 of each instruction byte 1-4 location are connected to a 4-input decoder 192 by lines 194. The output of decoder 192 is connected to memory controller 118 by line 196. Program counter 130 is connected to memory controller 118 by internal address bus 136, and the instruction register 108 is connected to the memory controller 118 by the internal data bus 90. Address/data bus 198 and control bus 200 are connected to the DRAMS 150 (FIG. 3).

In operation, when the most significant bits 190 of remaining instructions 1-4 are '1' in a clock cycle of the microprocessor 50, there are no memory reference instructions in the queue. The output of decoder 192 on line 196 requests an instruction fetch ahead by memory controller 118 without interference with other accesses. While the current instructions in instruction register 108 are executing, the memory controller 118 obtains the address of the next set of four instructions from program counter 130 and obtains that set of instructions. By the time the current set of instructions has completed execution, the next set of instructions is ready for loading into the instruction register.

Details of the DMA CPU 72 are provided in FIG. 5. Internal data bus 90 is connected to memory controller 118 and to DMA instruction register 210. The DMA instruction register 210 is connected to DMA program counter 212 by bus 214, to transfer size counter 216 by bus 218 and to timed transfer interval counter 220 by bus 222. The DMA instruction register 210 is also connected to DMA I/O and RAM address register 224 by line 226. The DMA I/O and RAM address register 224 is connected to the memory controller 118 by memory cycle request line 228 and bus 230. The DMA program counter 212 is connected to the internal address bus 136 by bus 232. The transfer size counter 216 is connected to a DMA instruction done decremter 234 by lines 236 and 238. The decremter 234 receives a control input on memory cycle acknowledge line 240. When trans-

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fer size counter 216 has completed its count, it provides a control signal to DMA program counter 212 on line 242. Timed transfer interval counter 220 is connected to decremter 244 by lines 246 and 248. The decremter 244 receives a control input from a microprocessor system clock on line 250.

The DMA CPU 72 controls itself and has the ability to fetch and execute instructions. It operates as a co-processor to the main CPU 70 (FIG. 2) for time specific processing.

FIG. 6 shows how the microprocessor 50 is connected to an electrically programmable read only memory (EPROM) 260 by reconfiguring the data lines 52 so that some of the data lines 52 are input lines and some of them are output lines. Data lines 52 D0-D7 provide data to and from corresponding data terminals 262 of the EPROM 260. Data lines 52 D9-D18 provide addresses to address terminals 264 of the EPROM 260. Data lines 52 D19-D31 provide inputs from the microprocessor 50 to memory and I/O decode logic 266. RAS 0/1 control line 268 provides a control signal for determining whether the memory and I/O decode logic provides a DRAM RAS output on line 270 or a column enable output for the EPROM 260 on line 272. Column address strobe terminal 60 of the microprocessor 50 provides an output enable signal on line 274 to the corresponding terminal 276 of the EPROM 260.

FIGS. 7 and 8 show the front and back of a one card data processing system 280 incorporating the microprocessor 50, MSM514258-10 type DRAMs 150 totalling 2 megabytes, a Motorola 50 MegaHertz crystal oscillator clock 282, I/O circuits 284 and a 27256 type EPROM 260. The I/O circuits 284 include a 74HC04 type high speed hex inverter circuit 286, an IDT39C828 type 10-bit inverting buffer circuit 288, an IDT39C822 type 10-bit inverting register circuit 290, and two IDT39C823 type 9-bit non-inverting register circuits 292. The card 280 is completed with a MAX12V type DC-DC converter circuit 294, 34-pin dual AMP type headers 296, a coaxial female power connector 298, and a 3-pin AMP right angle header 300. The card 280 is a low cost, imbeddable product that can be incorporated in larger systems or used as an internal development tool.

The microprocessor 50 is a very high performance (50 MHz) RISC influenced 32-bit CPU designed to work closely with dynamic RAM. Clock for clock, the microprocessor 50 approaches the theoretical performance limits possible with a single CPU configuration. Eventually, the microprocessor 50 and any other processor is limited by the bus bandwidth and the number of bus paths. The critical conduit is between the CPU and memory.

One solution to the bus bandwidth/bus path problem is to integrate a CPU directly onto the memory chips, giving every memory a direct bus to the CPU. FIG. 9 shows another microprocessor 310 that is provided integrally with 1 megabit of DRAM 311 in a single integrated circuit 312. Until the present invention, this solution has not been practical, because most high performance CPUs require from 500,000 to 1,000,000 transistors and enormous die sizes just by themselves. The microprocessor 310 is equivalent to the microprocessor 50 in FIGS. 1-8. The microprocessors 50 and 310 are the most transistor efficient high performance CPUs in existence, requiring fewer than 50,000 transistors for dual processors 70 and 72 (FIG. 2) or 314 and 316 (less memory). The very high speed of the microprocessors 50 and 310 is to a certain extent a function of the small number of active devices. In essence, the less silicon gets in the way, the faster the electrons can get where they are going.

The microprocessor 310 is therefore the only CPU suitable for integration on the memory chip die 312. Some

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simple modifications to the basic microprocessor 50 to take advantage of the proximity to the DRAM array 311 can also increase the microprocessor 50 clock speed by 50 percent, and probably more

The microprocessor 310 core on board the DRAM die 312 provides most of the speed and functionality required for a large group of applications from automotive to peripheral control. However, the integrated CPU 310/DRAM 311 concept has the potential to redefine significantly the way multiprocessor solutions can solve a spectrum of very compute intensive problems. The CPU 310/DRAM 311 combination eliminates the Von Neumann bottleneck by distributing it across numerous CPU/DRAM chips 312. The microprocessor 310 is a particularly good core for multiprocessing, since it was designed with the SDI targeting array in mind, and provisions were made for efficient interprocessor communications.

Traditional multiprocessor implementations have been very expensive in addition to being unable to exploit fully the available CPU horsepower. Multiprocessor systems have typically been built up from numerous board level or box level computers. The result is usually an immense amount of hardware with corresponding, wiring, power consumption, and communications problems. By the time the systems are interconnected, as much as 50 percent of the bus speed has been utilized just getting through the interfaces.

In addition, multiprocessor system software has been scarce. A multiprocessor system can easily be crippled by an inadequate load-sharing algorithm in the system software, which allows one CPU to do a great deal of work and the others to be idle. Great strides have been made recently in systems software, and even UNIX V.4 may be enhanced to support multiprocessing. Several commercial products from such manufacturers as DUAL Systems and UNISOFT do a credible job on 68030 type microprocessor systems now.

The microprocessor 310 architecture eliminates most of the interface friction, since up to 64 CPU 310 RAM 311 processors should be able to intercommunicate without buffers or latches. Each chip 312 has about 40 MIPS raw speed, because placing the DRAM 311 next to the CPU 310 allows the microprocessor 310 instruction cycle to be cut in half, compared to the microprocessor 50. A 64 chip array of these chips 312 is more powerful than any other existing computer. Such an array fits on a 3x5 card, cost less than a FAX machine, and draw about the same power as a small television.

Dramatic changes in price/performance always reshape existing applications and almost always create new ones. The introduction of microprocessors in the mid 1970s created video games, personal computers, automotive computers, electronically controlled appliances, and low cost computer peripherals.

The integrated circuit 312 will find applications in all of the above areas, plus create some new ones. A common generic parallel processing algorithm handles convolution/Fast Fourier Transform (FFT)/pattern recognition. Interesting product possibilities using the integrated circuit 312 include high speed reading machines, real-time speech recognition, spoken language translation, real-time robot vision, a product to identify people by their faces, and an automotive or aviation collision avoidance system.

A real time processor for enhancing high density television (HDTV) images, or compressing the HDTV information into a smaller bandwidth, would be very feasible. The load sharing in HDTV could be very straightforward. Splitting up the task according to color and frame would require 6, 9 or 12 processors. Practical implementation might require 4 meg RAMs integrated with the microprocessor 310.

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The microprocessor 310 has the following specifications:

CONTROL LINES

4—POWER/GROUND

1—CLOCK

32—DATA I/O

4—SYSTEM CONTROL

EXTERNAL MEMORY FETCH

EXTERNAL MEMORY FETCH AUTOINCREMENT X

EXTERNAL MEMORY FETCH AUTOINCREMENT Y

EXTERNAL MEMORY WRITE

EXTERNAL MEMORY WRITE AUTOINCREMENT X

EXTERNAL MEMORY WRITE AUTOINCREMENT Y

EXTERNAL PROM FETCH

LOAD ALL X REGISTERS

LOAD ALL Y REGISTERS

LOAD ALL PC REGISTERS

EXCHANGE X AND Y

INSTRUCTION FETCH

ADD TO PC

ADD TO X

WRITE MAPPING REGISTER

READ MAPPING REGISTER

REGISTER CONFIGURATION

MICROPROCESSOR 310 CPU 316 CORE

COLUMN LATCH1 (1024 BITS) 32x32 MUX

STACK POINTER (16 BITS)

COLUMN LATCH2 (1024 BITS) 32x32 MUX

RSTACK POINTER (16 BITS)

PROGRAM COUNTER 32 BITS

X0 REGISTER 32 BITS (ACTIVATED ONLY FOR ON-CHIP ACCESSES)

Y0 REGISTER 32 BITS (ACTIVATED ONLY FOR ON-CHIP ACCESSES)

LOOP COUNTER 32 BITS

DMA CPU 314 CORE

DMA PROGRAM COUNTER 24 BITS

INSTRUCTION REGISTER 32 BITS

I/O & RAM ADDRESS REGISTER 32 BITS

TRANSFER SIZE COUNTER 12 BITS

INTERVAL COUNTER 12 BITS

To offer memory expansion for the basic chip 312, an intelligent DRAM can be produced. This chip will be optimized for high speed operation with the integrated circuit 312 by having three on-chip address registers: Program Counter, X Register and Y register. As a result, to access the intelligent DRAM, no address is required, and a total access cycle could be as short as 10 nsec. Each expansion DRAM would maintain its own copy of the three registers and would be identified by a code specifying its memory address. Incrementing and adding to the three registers will actually take place on the memory chips. A maximum of 64 intelligent DRAM peripherals would allow a large system to be created without sacrificing speed by introducing multiplexers or buffers.

There are certain differences between the microprocessor 310 and the microprocessor 50 that arise from providing the microprocessor 310 on the same die 312 with the DRAM 311. Integrating the DRAM 311 allows architectural changes in the microprocessor 310 logic to take advantage of existing on-chip DRAM 311 circuitry. Row and column design is

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inherent in memory architecture. The DRAMs 311 access random bits in a memory array by first selecting a row of 1024 bits, storing them into a column latch, and then selecting one of the bits as the data to be read or written.

The time required to access the data is split between the row access and the column access. Selecting data already stored in a column latch is faster than selecting a random bit by at least a factor of six. The microprocessor 310 takes advantage of this high speed by creating a number of column latches and using them as caches and shift registers. Selecting a new row of information may be thought of as performing a 1024-bit read or write with the resulting immense bus bandwidth.

1 The microprocessor 50 treats its 32-bit instruction register 108 (see FIGS. 2 and 4) as a cache for four 8-bit instructions. Since the DRAM 311 maintains a 1024-bit latch for the column bits, the microprocessor 310 treats the column latch as a cache for 128 8-bit instructions. Therefore, the next instruction will almost always be already present in the cache. Long loops within the cache are also possible and more useful than the 4 instruction loops in the microprocessor 50.

2 The microprocessor 50 uses two 16x32-bit deep register arrays 74 and 134 (FIG. 2) for the parameter stack and the return stack. The microprocessor 310 creates two other 1024-bit column latches to provide the equivalent of two 32x32-bit arrays, which can be accessed twice as fast as a register array.

3 The microprocessor 50 has a DMA capability which can be used for I/O to a video shift register. The microprocessor 310 uses yet another 1024-bit column latch as a long video shift register to drive a CRT display directly. For color displays, three on-chip shift registers could also be used. These shift registers can transfer pixels at a maximum of 100 MHz.

4 The microprocessor 50 accesses memory via an external 32-bit bus. Most of the memory 311 for the microprocessor 310 is on the same die 312. External access to more memory is made using an 8-bit bus. The result is a smaller die, smaller package and lower power consumption than the microprocessor 50.

5 The microprocessor 50 consumes about a third of its operating power charging and discharging the I/O pins and associated capacitances. The DRAMs 150 (FIG. 8) connected to the microprocessor 50 dissipate most of their power in the I/O drivers. A microprocessor 310 system will consume about one-tenth the power of a microprocessor 50 system, since having the DRAM 311 next to the processor 310 eliminates most of the external capacitances to be charged and discharged.

6 Multiprocessing means splitting a computing task between numerous processors in order to speed up the solution. The popularity of multiprocessing is limited by the expense of current individual processors as well as the limited interprocessor communications ability. The microprocessor 310 is an excellent multiprocessor candidate, since the chip 312 is a monolithic computer complete with memory, rendering it low-cost and physically compact.

The shift registers implemented with the microprocessor 310 to perform video output can also be configured as interprocessor communication links. The INMOS transputer attempted a similar strategy, but at much lower speed and without the performance benefits inherent in the microprocessor 310 column latch architecture. Serial I/O is a prerequisite for many multiprocessor topologies because of the many neighbor processors which communicate. A cube has 6 neighbors. Each neighbor communicates using these lines:

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DATA IN
CLOCK IN
READY FOR DATA
DATA OUT
DATA READY?
CLOCK OUT

A special start up sequence is used to initialize the on-chip DRAM 311 in each of the processors.

The microprocessor 310 column latch architecture allows neighbor processors to deliver information directly to internal registers or even instruction caches of other chips 312. This technique is not used with existing processors, because it only improves performance in a tightly coupled DRAM system.

7 The microprocessor 50 architecture offers two types of looping structures: LOOP-IF-DONE and MICRO-LOOP. The former takes an 8-bit to 24-bit operand to describe the entry point to the loop address. The latter performs a loop entirely within the 4 instruction queue and the loop entry point is implied as the first instruction in the queue. Loops entirely within the queue run without external instruction fetches and execute up to three times as fast as the long loop construct. The microprocessor 310 retains both constructs with a few differences. The microprocessor 310 microloop functions in the same fashion as the microprocessor 50 operation, except the queue is 1024-bits or 128 8-bit instructions long. The microprocessor 310 microloop can therefore contain jumps, branches, calls and immediate operations not possible in the 4 8-bit instruction microprocessor 50 queue.

Microloops in the microprocessor 50 can only perform simple block move and compare functions. The larger microprocessor 310 queue allows entire digital signal processing or floating point algorithms to loop at high speed in the queue.

The microprocessor 50 offers four instructions to redirect execution:

CALL
BRANCH
BRANCH-IF-ZERO
LOOP-IF-NOT-DONE

These instructions take a variable length address operand 8, 16 or 24 bits long. The microprocessor 50 next address logic treats the three operands similarly by adding or subtracting them to the current program counter. For the microprocessor 310, the 16 and 24-bit operands function in the same manner as the 16 and 24-bit operands in the microprocessor 50. The 8-bit class operands are reserved to operate entirely within the instruction queue. Next address decisions can therefore be made quickly, because only 10 bits of addresses are affected, rather than 32. There is no carry or borrow generated past the 10 bits.

8 The microprocessor 310 CPU 316 resides on an already crowded DRAM die 312. To keep chip size as small as possible, the DMA processor 72 of the microprocessor 50 has been replaced with a more traditional DMA controller 314. DMA is used with the microprocessor 310 to perform the following functions:

Video output to a CRT
Multiprocessor serial communications
8-bit parallel I/O

The DMA controller 314 can maintain both serial and parallel transfers simultaneously. The following DMA sources and destinations are supported by the microprocessor 310:

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DESCRIPTION	I/O	LINES
1 Video shift register	OUTPUT	1 to 3
2 Multiprocessor serial	BOTH	6 lines/channel
3 8-bit parallel	BOTH	8 data, 4 control

The three sources use separate 1024-bit buffers and separate I/O pins. Therefore, all three may be active simultaneously without interference.

The microprocessor 310 can be implemented with either a single multiprocessor serial buffer or separate receive and sending buffers for each channel, allowing simultaneous bidirectional communications with six neighbors simultaneously.

FIGS 10 and 11 provide details of the PROM DMA used in the microprocessor 50. The microprocessor 50 executes faster than all but the fastest PROMs. PROMs are used in a microprocessor 50 system to store program segments and perhaps entire programs. The microprocessor 50 provides a feature on power-up to allow programs to be loaded from low-cost, slow speed PROMs into high speed DRAM for execution. The logic which performs this function is part of the DMA memory controller 118. The operation is similar to DMA, but not identical, since four 8-bit bytes must be assembled on the microprocessor 50 chip, then written to the DRAM 150.

The microprocessor 50 directly interfaces to DRAM 150 over a triple multiplexed data and address bus 350, which carries RAS addresses, CAS addresses and data. The EPROM 260, on the other hand, is read with non-multiplexed busses. The microprocessor 50 therefore has a special mode which unmultiplexes the data and address lines to read 8 bits of EPROM data. Four 8-bit bytes are read in this fashion. The multiplexed bus 350 is turned back on, and the data is written to the DRAM 150.

When the microprocessor 50 detects a RESET condition, the processor stops the main CPU 70 and forces a mode 0 (PROM LOAD) instruction into the DMA CPU 72 instruction register. The DMA instruction directs the memory controller to read the EPROM 260 data at 8 times the normal access time for memory. Assuming a 50 MHz microprocessor 50, this means an access time of 320 nsec. The instruction also indicates:

The selection address of the EPROM 260 to be loaded,

The number of 32-bit words to transfer,

The DRAM 150 address to transfer into

The sequence of activities to transfer one 32-bit word from EPROM 260 to DRAM 150 are:

1 RAS goes low at 352, latching the EPROM 260 select information from the high order address bits. The EPROM 260 is selected.

2 Twelve address bits (consisting of what is normally DRAM CAS addresses plus two byte select bits) are placed on the bus 350 going to the EPROM 260 address pins. These signals will remain on the lines until the data from the EPROM 260 has been read into the microprocessor 50. For the first byte, the byte select bits will be binary 00.

3 CAS goes low at 354 enabling the EPROM 260 data onto the lower 8 bits of the external address/data bus 350. NOTE: It is important to recognize that, during this part of the cycle, the lower 8 bits of the external data/address bus are functioning as inputs, but the rest of the bus is still acting as outputs.

4 The microprocessor 50 latches these eight least significant bits internally and shifts them 8 bits left to shift them to the next significant byte position.

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5 Steps 2, 3 and 4 are repeated with byte address 01

6 Steps 2, 3 and 4 are repeated with byte address 10

7 Steps 2, 3 and 4 are repeated with byte address 11

8 CAS goes high at 356, taking the EPROM 260 off the data bus

9. RAS goes high at 358, indicating the end of the EPROM 260 access

10 RAS goes low at 360, latching the DRAM select information from the high order address bits. At the same time, the RAS address bits are latched into the DRAM 150. The DRAM 150 is selected.

11 CAS goes low at 362, latching the DRAM 150 CAS addresses

12 The microprocessor 50 places the previously latched EPROM 260 32-bit data onto the external address/data bus 350. W goes low at 364, writing the 32 bits into the DRAM 150.

13 W goes high at 366. CAS goes high at 368. The process continues with the next word.

FIG. 12 shows details of the microprocessor 50 memory controller 118. In operation, bus requests stay present until they are serviced. CPU 70 requests are prioritized at 370 in the order of: 1, Parameter Stack; 2, Return Stack; 3, Data Fetch; 4, Instruction Fetch. The resulting CPU request signal and a DMA request signal are supplied as bus requests to bus control 372, which provides a bus grant signal at 374. Internal address bus 136 and a DMA counter 376 provide inputs to a multiplexer 378. Either a row address or a column address are provided as an output to multiplexed address bus 380 as an output from the multiplexer 378. The multiplexed address bus 380 and the internal data bus 90 provide address and data inputs, respectively, to multiplexer 382. Shift register 384 supplies row address strobe (RAS) 1 and 2 control signals to multiplexer 386 and column address strobe (CAS) 1 and 2 control signals to multiplexer 388 on lines 390 and 392. The shift register 384 also supplies output enable (OE) and write (W) signals on lines 394 and 396 and a control signal on line 398 to multiplexer 382. The shift register 384 receives a RUN signal on line 400 to generate a memory cycle and supplies a MEMORY READY signal on line 402 when an access is complete.

STACK/REGISTER ARCHITECTURE

Most microprocessors use on-chip registers for temporary storage of variables. The on-chip registers access data faster than off-chip RAM. A few microprocessors use an on-chip push down stack for temporary storage.

A stack has the advantage of faster operation compared to on-chip registers by avoiding the necessity to select source and destination registers. (A math or logic operation always uses the top two stack items as source and the top of stack as destination.) The stack's disadvantage is that it makes some operations clumsy. Some compiler activities in particular require on-chip registers for efficiency.

As shown in FIG. 13, the microprocessor 50 provides both on-chip registers 134 and a stack 74 and reaps the benefits of both.

BENEFITS:

1 Stack math and logic is twice as fast as those available on an equivalent register only machine. Most programmers and optimizing compilers can take advantage of this feature.

2 Sixteen registers are available for on-chip storage of local variables which can transfer to the stack for computation. The accessing of variables is three to four times as fast as available on a strictly stack machine.

The combined stack 74/register 134 architecture has not been used previously due to inadequate understanding by computer designers of optimizing compilers and the mix of transfer versus math/logic instructions.

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ADAPTIVE MEMORY CONTROLLER

A microprocessor must be designed to work with small or large memory configurations. As more memory loads are added to the data address, and control lines, the switching speed of the signals slows down. The microprocessor 50 multiplexes the address/data bus three ways, so timing between the phases is critical. A traditional approach to the problem allocates a wide margin of time between bus phases so that systems will work with small or large numbers of memory chips connected. A speed compromise of as much as 50% is required.

As shown in FIG 14, the microprocessor 50 uses a feedback technique to allow the processor to adjust memory bus timing to be fast with small loads and slower with large ones. The OUTPUT ENABLE (OE) line 152 from the microprocessor 50 is connected to all memories 150 on the circuit board. The loading on the output enable line 152 to the microprocessor 50 is directly related to the number of memories 150 connected. By monitoring how rapidly OE 152 goes high after a read, the microprocessor 50 is able to determine when the data hold time has been satisfied and place the next address on the bus.

The level of the OE line 152 is monitored by CMOS input buffer 410 which generates an internal READY signal on line 412 to the microprocessor's memory controller. Curves 414 and 416 of the FIG 15 graph show the difference in rise time likely to be encountered from a lightly to heavily loaded memory system. When the OE line 152 has reached a predetermined level to generate the READY signal, driver 418 generates an OUTPUT ENABLE signal on OE line 152.

SKIP WITHIN THE INSTRUCTION CACHE

The microprocessor 50 fetches four 8-bit instructions each memory cycle and stores them in a 32-bit instruction register 108, as shown in FIG 16. A class of "test and skip" instructions can very rapidly execute a very fast jump operation within the four instruction cache.

SKIP CONDITIONS:

Always
ACC non-zero
ACC negative
Carry flag equal logic one
Never
ACC equal zero
ACC positive
Carry flag equal logic zero

The SKIP instruction can be located in any of the four byte positions 420 in the 32-bit instruction register 108. If the test is successful, SKIP will jump over the remaining one, two, or three 8-bit instructions in the instruction register 108 and cause the next four-instruction group to be loaded into the register 108.

As shown, the SKIP operation is implemented by resetting the 2-bit microinstruction counter 180 to zero on line 422 and simultaneously latching the next instruction group into the register 108. Any instructions following the SKIP in the instruction register are overwritten by the new instructions and not executed.

The advantage of SKIP is that optimizing compilers and smart programmers can often use it in place of the longer conditional JUMP instruction. SKIP also makes possible microloops which exit when the loop counts down or when the SKIP jumps to the next instruction group. The result is very fast code.

Other machines (such as the PDP-8 and Data General NOVA) provide the ability to skip a single instruction. The microprocessor 50 provides the ability to skip up to three instructions.

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MICROLOOP IN THE INSTRUCTION CACHE

The microprocessor 50 provides the MICROLOOP instruction to execute repetitively from one to three instructions residing in the instruction register 108. The microloop instruction works in conjunction with the LOOP COUNTER 92 (FIG 2) connected to the internal data bus 90. To execute a microloop, the program stores a count in LOOP COUNTER 92. MICROLOOP may be placed in the first, second, third, or last byte 420 of the instruction register 108.

If placed in the first position, execution will just create a delay equal to the number stored in LOOP COUNTER 92 times the machine cycle. If placed in the second, third, or last byte 420, when the microloop instruction is executed, it will test the LOOP COUNT for zero. If zero, execution will continue with the next instruction. If not zero, the LOOP COUNTER 92 is decremented and the 2-bit microinstruction counter is cleared, causing the preceding instructions in the instruction register to be executed again.

Microloop is useful for block move and search operations. By executing a block move completely out of the instruction register 108, the speed of the move is doubled, since all memory cycles are used by the move rather than being shared with instruction fetching. Such a hardware implementation of microloops is much faster than conventional software implementation of a comparable function.

OPTIMAL CPU CLOCK SCHEME

The designer of a high speed microprocessor must produce a product which operate over wide temperature ranges, wide voltage swings, and wide variations in semiconductor processing. Temperature, voltage, and process all affect transistor propagation delays. Traditional CPU designs are done so that with the worse case of the three parameters, the circuit will function at the rated clock speed. The result are designs that must be clocked a factor of two slower than their maximum theoretical performance, so they will operate properly in worse case conditions.

The microprocessor 50 uses the technique shown in FIGS 17-19 to generate the system clock and its required phases. Clock circuit 430 is the familiar "ring oscillator" used to test process performance. The clock is fabricated on the same silicon chip as the rest of the microprocessor 50.

The ring oscillator frequency is determined by the parameters of temperature, voltage, and process. At room temperature, the frequency will be in the neighborhood of 100 MHz. At 70 degrees Centigrade, the speed will be 50 MHz. The ring oscillator 430 is useful as a system clock, with its stages 431 producing phase 0-phase 3 outputs 433 shown in FIG 19, because its performance tracks the parameters which similarly affect all other transistors on the same silicon die. By deriving system timing from the ring oscillator 430, CPU 70 will always execute at the maximum frequency possible, but never too fast. For example, if the processing of a particular die is not good resulting in slow transistors, the latches and gates on the microprocessor 50 will operate slower than normal. Since the microprocessor 50 ring oscillator clock 430 is made from the same transistors on the same die as the latches and gates, it too will operate slower (oscillating at a lower frequency), providing compensation which allows the rest of the chip's logic to operate properly.

ASYNCHRONOUS/SYNCHRONOUS CPU

Most microprocessors derive all system timing from a single clock. The disadvantage is that different parts of the system can slow all operations. The microprocessor 50 provides a dual-clock scheme as shown in FIG 17, with the CPU 70 operating asynchronously to I/O interface 432 forming part of memory controller 118 (FIG 2) and the I/O

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interface 432 operating synchronously with the external world of memory and I/O devices. The CPU 70 executes at the fastest speed possible using the adaptive ring counter clock 430. Speed may vary by a factor of four depending upon temperature, voltage, and process. The external world must be synchronized to the microprocessor 50 for operations such as video display updating and disc drive reading and writing. This synchronization is performed by the I/O interface 432, speed of which is controlled by a conventional crystal clock 434. The interface 432 processes requests for memory accesses from the microprocessor 50 and acknowledges the presence of I/O data. The microprocessor 50 fetches up to four instructions in a single memory cycle and can perform much useful work before requiring another memory access. By decoupling the variable speed of the CPU 70 from the fixed speed of the I/O interface 432, optimum performance can be achieved by each. Recoupling between the CPU 70 and the interface 432 is accomplished with handshake signals on lines 436, with data/addresses passing on bus 90, 136.

ASYNCHRONOUS/SYNCHRONOUS CPU IMBEDDED ON A DRAM CHIP

System performance is enhanced even more when the DRAM 311 and CPU 314 (FIG. 9) are located on the same die. The proximity of the transistors means that DRAM 311 and CPU 314 parameters will closely follow each other. At room temperature, not only would the CPU 314 execute at 100 MHz, but the DRAM 311 would access fast enough to keep up. The synchronization performed by the I/O interface 432 would be for DMA and reading and writing I/O ports. In some systems (such as calculators) no I/O synchronization at all would be required, and the I/O clock would be tied to the ring counter clock.

VARIABLE WIDTH OPERANDS

Many microprocessors provide variable width operands. The microprocessor 50 handles operands of 8, 16, or 24 bits using the same op-code. FIG. 20 shows the 32-bit instruction register 108 and the 2-bit microinstruction register 180 which selects the 8-bit instruction. Two classes of microprocessor 50 instructions can be greater than 8-bits, JUMP class and IMMEDIATE. A JUMP or IMMEDIATE op-code is 8-bits, but the operand can be 8, 16, or 24 bits long. This magic is possible because operands must be right justified in the instruction register. This means that the least significant bit of the operand is always located in the least significant bit of the instruction register. The microinstruction counter 180 selects which 8-bit instruction to execute. If a JUMP or IMMEDIATE instruction is decoded, the state of the 2-bit microinstruction counter selects the required 8, 16, or 24 bit operand onto the address or data bus. The unselected 8-bit bytes are loaded with zeros by operation of decoder 440 and gates 442. The advantage of this technique is the saving of a number of op-codes required to specify the different operand sizes in other microprocessors.

TRIPLE STACK CACHE

Computer performance is directly related to the system memory bandwidth. The faster the memories, the faster the computer. Fast memories are expensive, so techniques have been developed to move a small amount of high-speed memory around to the memory addresses where it is needed. A large amount of slow memory is constantly updated by the fast memory, giving the appearance of a large fast memory array. A common implementation of the technique is known as a high-speed memory cache. The cache may be thought of as fast acting shock absorber smoothing out the bumps in memory access. When more memory is required than the shock can absorb, it bottoms out and slow speed memory is

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accessed. Most memory operations can be handled by the shock absorber itself. The microprocessor 50 architecture has the ALU 80 (FIG. 2) directly coupled to the top two stack locations 76 and 78. The access time of the stack 74 therefore directly affects the execution speed of the processor. The microprocessor 50 stack architecture is particularly suitable to a triple cache technique, shown in FIG. 21 which offers the appearance of a large stack memory operating at the speed of on-chip latches 450. Latches 450 are the fastest form of memory device built on the chip, delivering data in as little as 3 nsec. However latches 450 require large numbers of transistors to construct. On-chip RAM 452 requires fewer transistors than latches, but is slower by a factor of five (15 nsec access). Off-chip RAM 150 is the slowest storage of all. The microprocessor 50 organizes the stack memory hierarchy as three interconnected stacks 450, 452 and 454. The latch stack 450 is the fastest and most frequently used. The on-chip RAM stack 452 is next. The off-chip RAM stack 454 is slowest. The stack modulation determines the effective access time of the stack. If a group of stack operations never push or pull more than four consecutive items on the stack, operations will be entirely performed in the 3 nsec latch stack. When the four latches 456 are filled, the data in the bottom of the latch stack 450 is written to the top of the on-chip RAM stack 452. When the sixteen locations 458 in the on-chip RAM stack 452 are filled, the data in the bottom of the on-chip RAM stack 452 is written to the top of the off-chip RAM stack 454. When popping data off a full stack 450, four pops will be performed before stack empty line 460 from the latch stack pointer 462 transfers data from the on-chip RAM stack 452. By waiting for the latch stack 450 to empty before performing the slower on-chip RAM access, the high effective speed of the latches 456 are made available to the processor. The same approach is employed with the on-chip RAM stack 452 and the off-chip RAM stack 454.

POLYNOMIAL GENERATION INSTRUCTION

Polynomials are useful for error correction, encryption, data compression, and fractal generation. A polynomial is generated by a sequence of shift and exclusive OR operations. Special chips are provided for this purpose in the prior art.

The microprocessor 50 is able to generate polynomials at high speed without external hardware by slightly modifying how the ALU 80 works. As shown in FIG. 22, a polynomial is generated by loading the "order" (also known as the feedback terms) into C Register 470. The value thirty one (resulting in 32 iterations) is loaded into DOWN COUNTER 472. A register 474 is loaded with zero. B register 476 is loaded with the starting polynomial value. When the POLY instruction executes, C register 470 is exclusively ORed with A register 474 if the least significant bit of B register 476 is a one. Otherwise, the contents of the A register 474 passes through the ALU 80 unaltered. The combination of A and B is then shifted right (divided by 2) with shifters 478 and 480. The operation automatically repeats the specified number of iterations, and the resulting polynomial is left in A register 474.

FAST MULTIPLY

Most microprocessors offer a 16x16 or 32x32 bit multiply instruction. Multiply when performed sequentially takes one shift/add per bit, or 32 cycles for 32 bit data. The microprocessor 50 provides a high speed multiply which allows multiplication by small numbers using only a small number of cycles. FIG. 23 shows the logic used to implement the high speed algorithm. To perform a multiply, the size of the multiplier less one is placed in the DOWN COUNTER 472.

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For a four bit multiplier, the number three would be stored in the DOWN COUNTER 472. Zero is loaded into the A register 474. The multiplier is written bit reversed into the B Register 476. For example, a bit reversed five (binary 0101) would be written into B as 1010. The multiplicand is written into the C register 470. Executing the FAST MULT instruction will leave the result in the A Register 474, when the count has been completed. The fast multiply instruction is important because many applications scale one number by a much smaller number. The difference in speed between multiplying a 32x32 bit and a 32x4 bit is a factor of 8. If the least significant bit of the multiplier is a "ONE", the contents of the A register 474 and the C register 470 are added. If the least significant bit of the multiplier is a "ZERO", the contents of the A register are passed through the ALU 80 unaltered. The output of the ALU 80 is shifted left by shifter 482 in each iteration. The contents of the B register 476 are shifted right by the shifter 480 in each iteration.

INSTRUCTION EXECUTION PHILOSOPHY

The microprocessor 50 uses high speed D latches in most of the speed critical areas. Slower on-chip RAM is used as secondary storage.

The microprocessor 50 philosophy of instruction execution is to create a hierarchy of speed as follows:

Logic and D latch transfers	1 cycle	20 nsec
Math	2 cycles	40 nsec
Fetch/store on-chip RAM	2 cycles	40 nsec
Fetch/store in current RAS page	4 cycles	80 nsec
Fetch/store with RAS cycle	11 cycles	220 nsec

With a 50 MHZ clock, many operations can be performed in 20 nsec. and almost everything else in 40 nsec.

To maximize speed, certain techniques in processor design have been used. They include:

- Eliminating arithmetic operations on addresses,
- Fetching up to four instructions per memory cycle,
- Pipelineless instruction decoding
- Generating results before they are needed,
- Use of three level stack caching

PIPELINE PHILOSOPHY

Computer instructions are usually broken down into sequential pieces, for example: fetch, decode, register read, execute, and store. Each piece will require a single machine cycle. In most Reduced Instruction Set Computer (RISC) chips, instruction require from three to six cycles.

RISC instructions are very parallel. For example, each of 70 different instructions in the SPARC (SUN Computer's RISC chip) has five cycles. Using a technique called "pipelining", the different phases of consecutive instructions can be overlapped.

To understand pipelining, think of building five residential homes. Each home will require in sequence, a foundation, framing, plumbing and wiring, roofing, and interior finish. Assume that each activity takes one week. To build one house will take five weeks.

But what if you want to build an entire subdivision? You have only one of each work crew, but when the foundation men finish on the first house, you immediately start them on the second one, and so on. At the end of five weeks, the first home is complete, but you also have five foundations. If you have kept the framing, plumbing, roofing, and interior guys all busy, from five weeks on, a new house will be completed each week.

This is the way a RISC chip like SPARC appears to execute an instruction in a single machine cycle. In reality,

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a RISC chip is executing one fifth of five instructions each machine cycle. And if five instructions stay in sequence, an instruction will be completed each machine cycle.

The problems with a pipeline are keeping the pipe full with instructions. Each time an out of sequence instruction such as a BRANCH or CALL occurs, the pipe must be refilled with the next sequence. The resulting dead time to refill the pipeline can become substantial when many IF/THEN/ELSE statements or subroutines are encountered.

THE PIPELINE APPROACH

The microprocessor 50 has no pipeline as such. The approach of this microprocessor to speed is to overlap instruction fetching with execution of the previously fetched instruction(s). Beyond that, over half the instructions (the most common ones) execute entirely in a single machine cycle of 20 nsec. This is possible because:

- 1 Instruction decoding resolves in 2.5 nsec
- 2 Incremented/decremented and some math values are calculated before they are needed, requiring only a latching signal to execute.
- 3 Slower memory is hidden from high speed operations by high-speed D latches which access in 4 nsec. The disadvantage for this microprocessor is a more complex chip design process. The advantage for the chip user is faster ultimate throughput since pipeline stalls cannot exist. Pipeline synchronization with availability flag bits and other such pipeline handling is not required by this microprocessor.

For example, in some RISC machines an instruction which tests a status flag may have to wait for up to four cycles for the flag set by the previous instruction to be available to be tested. Hardware and software debugging is also somewhat easier because the user doesn't have to visualize five instructions simultaneously in the pipe.

OVERLAPPING INSTRUCTION FETCH/EXECUTE

The slowest procedure the microprocessor 50 performs is to access memory. Memory is accessed when data is read or written. Memory is also read when instructions are fetched. The microprocessor 50 is able to hide fetch of the next instruction behind the execution of the previously fetched instruction(s). The microprocessor 50 fetches instructions in 4-byte instruction groups. An instruction group may contain from one to four instructions. The amount of time required to execute the instruction group ranges from 4 cycles for simple instructions to 64 cycles for a multiply.

When a new instruction group is fetched, the microprocessor instruction decoder looks at the most significant bit of all four of the bytes. The most significant bit of an instruction determines if a memory access is required. For example, CALL, FETCH, and STORE all require a memory access to execute. If all four bytes have nonzero most significant bits, the microprocessor initiates the memory fetch of the next sequential 4-byte instruction group. When the last instruction in the group finishes executing, the next 4-byte instruction group is ready and waiting on the data bus needing only to be latched into the instruction register. If the 4-byte instruction group required four or more cycles to execute and the next sequential access was a column address strobe (CAS) cycle, the instruction fetch was completely overlapped with execution.

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INTERNAL ARCHITECTURE

The microprocessor 50 architecture consists of the following:

PARAMETER STACK <-->	Y REGISTER RETURN STACK
ALU	
<--32 BITS--> 16 DEEP	<--32 BITS--> 16 DEEP
Used for math and logic	Used for subroutine and interrupt return addresses as well as local variables
Push down stack.	Push down stack
Can overflow into off-chip RAM.	Can overflow into off-chip RAM
LOOP COUNTER	Can also be accessed relative to top of stack (32-bits, can decrement by 1)
X REGISTER	Used by class of test and loop instructions (32-bits, can increment or decrement by 4)
PROGRAM COUNTER	Used to point to RAM locations (32-bits, increments by 4) Points to 4-byte instruction groups in RAM
INSTRUCTION REG	(32-Bits) Holds 4-byte instruction groups while they are being decoded and executed

*Math and logic operations use the TOP item and NEXT to top Parameter Stack items as the operands. The result is pushed onto the Parameter Stack.

*Return addresses from subroutines are placed on the Return Stack. The Y REGISTER is used as a pointer to RAM locations. Since the Y REGISTER is the top item of the Return Stack, nesting of indices is straightforward.

MODE—A register with mode and status bits

MODE-BITS:

- Slow down memory accesses by 8 if "1". Run full speed if "0". (Provided for access to slow EPROM.)
- Divide the system clock by 1023 if "1" to reduce power consumption. Run full speed if "0". (On-chip counters slow down if this bit is set.)
- Enable external interrupt 1
- Enable external interrupt 2
- Enable external interrupt 3
- Enable external interrupt 4
- Enable external interrupt 5
- Enable external interrupt 6
- Enable external interrupt 7.

ON-CHIP MEMORY LOCATIONS:

MODE-BITS

DMA-POINTER

DMA-COUNTER

STACK-POINTER—Pointer into Parameter Stack

STACK-DEPTH—Depth of on-chip Parameter Stack

RSTACK-POINTER—Pointer into Return Stack

RSTACK-DEPTH—Depth of on-chip Return Stack

ADDRESSING MODE HIGH POINTS

The data bus is 32-bits wide. All memory fetches and stores are 32-bits. Memory bus addresses are 30 bits. The least significant 2 bits are used to select one-of-four bytes in some addressing modes. The Program Counter, X Register, and Y Register are implemented as D latches with their outputs going to the memory address bus and the bus incrementer/decrementer. Incrementing one of these registers can happen quickly, because the incremented value has already rippled through the inc/dec logic and need only be clocked into the latch. Branches and Calls are made to 32-bit word boundaries.

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INSTRUCTION SET

32-BIT INSTRUCTION FORMAT

The thirty two bit instructions are CALL, BRANCH, BRANCH-IF-ZERO, and LOOP-IF-NOT-DONE. These instructions require the calculation of an effective address. In many computers, the effective address is calculated by adding or subtracting an operand with the current Program Counter. This math operation requires from four to seven machine cycles to perform and can definitely bog down machine execution. The microprocessor's strategy is to perform the required math operation at assembly or linking time and do a much simpler "Increment to next page" or "Decrement to previous page" operation at run time. As a result, the microprocessor branches execute in a single cycle.

24-BIT OPERAND FORM

Byte 1	Byte 2	Byte 3	Byte 4
WWWWWW XX	YYYYYYYY	YYYYYYYY	YYYYYYYY

With a 24-bit operand, the current page is considered to be defined by the most significant 6 bits of the Program Counter.

16-BIT OPERAND FORM:

With a 16-bit operand, the current page is considered to be defined by the most significant 14 bits of the Program Counter.

8-BIT OPERAND FORM:

With an 8-bit operand, the current page is considered to be defined by the most significant 22 bits of the Program Counter.

Any 8-bit instruction

WWWWWW—Instruction op-code

XX—Select how the address bits will be used:

00 —Make all high-order bits zero. (Page zero addressing)

01 —Increment the high-order bits (Use next page)

10 —Decrement the high-order bits (Use previous page)

11 —Leave the high-order bits unchanged (Use current page)

YYYYYYYY —The address operand field. This field is always shifted left two bits (to generate a word rather than byte address) and loaded into the Program Counter. The microprocessor instruction decoder figures out the width of the operand field by the location of the instruction op-code in the four bytes.

The compiler or assembler will normally use the shortest operand required to reach the desired address so that the leading bytes can be used to hold other instructions. The effective address is calculated by combining:

The current Program Counter,

The 8, 16, or 24 bit address operand in the instruction,

Using one of the four allowed addressing modes.

EXAMPLES OF EFFECTIVE ADDRESS CALCULATION

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EXAMPLE 1

Byte 1	Byte 2	Byte 3	Byte 4
QQQQQQQQ	QQQQQQQQ	00000011	10011000

The "QQQQQQQQs" in Byte 1 and 2 indicate space in the 4-byte memory fetch which could be hold two other instructions to be executed prior to the CALL instruction. Byte 3 indicates a CALL instruction (six zeros) in the current page (indicated by the 11 bits). Byte 4 indicates that the hexadecimal number 98 will be forced into the Program Counter bits 2 through 10 (Remember, a CALL or BRANCH always goes to a word boundary so the two least significant bits are always set to zero). The effect of this instruction would be to CALL a subroutine at WORD location HEX 98 in the current page. The most significant 22 bits of the Program Counter define the current page and will be unchanged.

EXAMPLE 2

Byte 1	Byte 2	Byte 3	Byte 4
000001 01	00000001	00000000	00000000

If we assume that the Program Counter was HEX 0000 0156 which is binary: 00000000 00000000 00000001 01010110 = OLD PROGRAM COUNTER. Byte 1 indicates a BRANCH instruction op code (000001) and "01" indicates select the next page. Byte 2, 3, and 4 are the address operand. These 24-bits will be shifted to the left two places to define a WORD address. HEX 0156 shifted left two places is HEX 0558. Since this is a 24-bit operand instruction, the most significant 6 bits of the Program Counter define the current page. These six bits will be incremented to select the next page. Executing this instruction will cause the Program Counter to be loaded with HEX 0400 0558 which is binary:

00000100 00000000 00000101 01011000 = NEW PROGRAM COUNTER
INSTRUCTIONS
CALL-LONG

0000 00XX - YYYYYYYYYY - YYYYYYYYYY - YYYYYYYYYY

Load the Program Counter with the effective WORD address specified. Push the current PC contents onto the RETURN STACK.

OTHER EFFECTS: CARRY or modes, no effect. May cause Return Stack to force an external memory cycle if on-chip Return Stack is full.

BRANCH

0000 01XX - YYYYYYYYYY - YYYYYYYYYY - YYYYYYYYYY

Load the Program Counter with the effective WORD address specified.

OTHER EFFECTS: NONE

BRANCH-IF-ZERO

0000 10XX - YYYYYYYYYY - YYYYYYYYYY - YYYYYYYYYY

Test the TOP value on the Parameter Stack. If the value is equal to zero, load the Program Counter with the effective WORD address specified. If the TOP value is not equal to zero, increment the Program Counter and fetch and execute the next instruction.

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OTHER EFFECTS: NONE

LOOP-IF-NOT-DONE

0000 11 YY - (XXXX XXXX) - (XXXX XXXX) - (XXXX XXXX)

If the LOOP COUNTER is not zero, load the Program Counter with the effective WORD address specified. If the LOOP COUNTER is zero, decrement the LOOP COUNTER, increment the Program Counter and fetch and execute the next instruction.

OTHER EFFECTS: NONE

8-BIT INSTRUCTIONS PHILOSOPHY

Most of the work in the microprocessor 50 is done by the 8-bit instructions. Eight bit instructions are possible with the microprocessor because of the extensive use of implied stack addressing. Many 32-bit architectures use 8-bits to specify the operation to perform but use an additional 24-bits to specify two sources and a destination.

For math and logic operations, the microprocessor 50 exploits the inherent advantage of a stack by designating the source operand(s) as the top stack item and the next stack item. The math or logic operation is performed, the operands are popped from the stack, and the result is pushed back on the stack. The result is a very efficient utilization of instruction bits as well as registers. A comparable situation exists between Hewlett Packard calculators (which use a stack) and Texas Instrument calculators which don't. The identical operation on an HP will require one half to one third the keystrokes of the TI.

The availability of 8-bit instructions also allows another architectural innovation, the fetching of four instructions in a single 32-bit memory cycle. The advantages of fetching multiple instructions are:

Increased execution speed even with slow memories.

Similar performance to the Harvard (separate data and instruction busses) without the expense,

Opportunities to optimize groups of instructions.

The capability to perform loops within this mini-cache.

The microloops inside the four instruction group are effective for searches and block moves.

SKIP INSTRUCTIONS

The microprocessor 50 fetches instructions in 32-bit chunks called 4-byte instruction groups. These four bytes may contain four 8-bit instructions or some mix of 8-bit and 16 or 24-bit instructions. SKIP instructions in the microprocessor skip any remaining instructions in a 4-byte instruction group and cause a memory fetch to get the next 4-byte instruction group.

Conditional SKIPS when combined with 3-byte BRANCHES will create conditional BRANCHES. SKIPS may also be used in situations when no use can be made of the remaining bytes in a 4-instruction group. A SKIP executes in a single cycle, whereas a group of three NOPs would take three cycles.

SKIP-ALWAYS—Skip any remaining instructions in this 4-byte instruction group.

Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group.

SKIP-IF-ZERO—If the TOP item of the Parameter Stack is zero, skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group.

If the TOP item is not zero, execute the next sequential instruction.

SKIP-IF-POSITIVE—If the TOP item of the Parameter Stack has a the most significant bit (the sign bit) equal to '0', skip any remaining instructions in the 4-byte instruction group.

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group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the TOP item is not '0', execute the next sequential instruction.

SKIP-IF-NO-CARRY—If the CARRY flag from a SHIFT or arithmetic operation is not equal to "1", skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the CARRY is equal to "1", execute the next sequential instruction.

SKIP-NEVER—Execute the next sequential (NOP) instruction. (Delay one machine cycle).

SKIP-IF-NOT-ZERO - If the TOP item on the Parameter Stack is not equal to "0", skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group.

If the TOP item is equal "0", execute the next sequential instruction.

SKIP-IF-NEGATIVE—If the TOP item on the Parameter Stack has its most significant bit (sign bit) set to "1", skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the TOP item has its most significant bit set to "0", execute the next sequential instruction.

SKIP-IF-CARRY—If the CARRY flag is set to "1" as a result of SHIFT or arithmetic operation, skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the CARRY flag is "0", execute the next sequential instruction.

MICROLOOPS

Microloops are a unique feature of the microprocessor architecture which allows controlled looping within a 4-byte instruction group. A microloop instruction tests the LOOP COUNTER for "0" and may perform an additional test. If the LOOP COUNTER is not "0" and the test is met, instruction execution continues with the first instruction in the 4-byte instruction group, and the LOOP COUNTER is decremented. A microloop instruction will usually be the last byte in a 4-byte instruction group, but it can be any byte. If the LOOP COUNTER is "0" or the test is not met, instruction execution continues with the next instruction. If the microloop is the last byte in the 4-byte instruction group, the most significant 30-bits of the Program Counter are incremented and the next 4-byte instruction group is fetched from memory. On a termination of the loop on LOOP COUNTER equal to "0", the LOOP COUNTER will remain at "0". Microloops allow short iterative work such as moves and searches to be performed without slowing down to fetch instructions from memory.

EXAMPLE

Byte 1 FETCH-VIA-X-AUTOINCREMENT	Byte 2 STORE-VIA-Y-AUTOINCREMENT
Byte 3 ULoop-UNTIL-DONE	Byte 4 QQQQQQQQ

This example will perform a block move. To initiate the transfer, X will be loaded with the starting address of the source. Y will be loaded with the starting address of the

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destination. The LOOP COUNTER will be loaded with the number of 32-bit words to move. The microloop will FETCH and STORE and count down the LOOP COUNTER until it reaches zero. QQQQQQQQ indicates any instruction can follow.

MICROLOOP INSTRUCTIONS

ULoop-UNTIL-DONE—If the LOOP COUNTER is not "0", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0", continue execution with the next instruction.

ULoop-IF-ZERO—If the LOOP COUNTER is not "0" and the TOP item on the Parameter Stack is "0", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the TOP item is "1", continue execution with the next instruction.

ULoop-IF-POSITIVE—If the LOOP COUNTER is not "0" and the most significant bit (sign bit) is "0", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the TOP item is "1", continue execution with the next instruction.

ULoop-IF-NOT-CARRY-CLEAR—If the LOOP COUNTER is not "0" and the floating point exponents found in TOP and NEXT are not aligned, continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the exponents are aligned, continue execution with the next instruction.

This instruction is specifically designed for combination with special SHIFT instructions to align two floating point numbers.

ULoop-NEVER—(DECREMENT-LOOP-COUNTER) Decrement the LOOP COUNTER. Continue execution with the next instruction.

ULoop-IF-NOT-ZERO—If the LOOP COUNTER is not "0" and the TOP item of the Parameter Stack is "0", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the TOP item is "1", continue execution with the next instruction.

ULoop-IF-NEGATIVE—If the LOOP COUNTER is not "0" and the most significant bit (sign bit) of the TOP item of the Parameter Stack is "1", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the most significant bit of the Parameter Stack is "0", continue execution with the next instruction.

ULoop-IF-CARRY-SET—If the LOOP COUNTER is not "0" and the exponents of the floating point numbers

found in TOP and NEXT are not aligned, continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the

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LOOP COUNTER is "0" or the exponents are aligned continue execution with the next instruction.

RETURN FROM SUBROUTINE OR INTERRUPT

Subroutine calls and interrupt acknowledgements cause a redirection of normal program execution. In both cases, the current Program Counter is pushed onto the Return Stack, so the microprocessor can return to its place in the program after executing the subroutine or interrupt service routine.

NOTE: When a CALL to subroutine or interrupt is acknowledged the Program Counter has already been incremented and is pointing to the 4-byte instruction group following the 4-byte group currently being executed. The instruction decoding logic allows the microprocessor to perform a test and execute a return conditional on the outcome of the test in a single cycle. A RETURN pops an address from the Return Stack and stores it to the Program Counter.

RETURN INSTRUCTIONS

RETURN-ALWAYS—Pop the top item from the Return Stack and transfer it to the Program Counter.

RETURN-IF-ZERO—If the TOP item on the Parameter Stack is "0", pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-IF-POSITIVE—If the most significant bit (sign bit) of the TOP item on the Parameter Stack is a "0", pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-IF-CARRY-CLEAR—If the exponents of the floating point numbers found in TOP and NEXT are not aligned, pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-NEVER—Execute the next instruction (NOP).

RETURN-IF-NOT-ZERO—If the TOP item on the Parameter Stack is not "0", pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-IF-NEGATIVE—If the most significant bit (sign bit) of the TOP item on the Parameter Stack is a "1", pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-IF-CARRY-SET—If the exponents of the floating point numbers found in TOP and NEXT are aligned, pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

HANDLING MEMORY FROM DYNAMIC RAM

The microprocessor 50, like any RISC type architecture, is optimized to handle as many operations as possible on-chip for maximum speed. External memory operations take from 80 nsec. to 220 nsec. compared with on-chip memory speeds of from 4 nsec. to 30 nsec. There are times when external memory must be accessed.

External memory is accessed using three registers:

X-REGISTER—A 30-bit memory pointer which can be used for memory access and simultaneously incremented or decremented.

Y-REGISTER—A 30-bit memory pointer which can be used for memory access and simultaneously incremented or decremented.

PROGRAM-COUNTER—A 30-bit memory pointer normally used to point to 4-byte instruction groups. Exter-

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nal memory may be accessed at addresses relative to the PC. The operands are sometimes called "Immediate" or "Literal" in other computers. When used as memory pointer, the PC is also incremented after each operation.

MEMORY LOAD & STORE INSTRUCTIONS

FEICH-VIA-X—Fetch the 32-bit memory content pointed to by X and push it onto the Parameter Stack. X is unchanged.

FEICH-VIA-Y—Fetch the 32-bit memory content pointed to by Y and push it onto the Parameter Stack. Y is unchanged.

FEICH-VIA-X-AUTOINCREMENT—Fetch the 32-bit memory content pointed to by X and push it onto the Parameter Stack. After fetching, increment the most significant 30 bits of X to point to the next 32-bit word address.

FEICH-VIA-Y-AUTOINCREMENT—Fetch the 32-bit memory content pointed to by Y and push it onto the Parameter Stack. After fetching, increment the most significant 30 bits of Y to point to the next 32-bit word address.

FEICH-VIA-X-AUTODECREMENT—Fetch the 32-bit memory content pointed to by X and push it onto the Parameter Stack. After fetching, decrement the most significant 30 bits of X to point to the previous 32-bit word address.

FEICH-VIA-Y-AUTODECREMENT—Fetch the 32-bit memory content pointed to by Y and push it onto the Parameter Stack. After fetching, decrement the most significant 30 bits of Y to point to the previous 32-bit word address.

STORE-VIA-X—Pop the top item of the Parameter Stack and store it in the memory location pointed to by X. X is unchanged.

STORE-VIA-Y—Pop the top item of the Parameter Stack and store it in the memory location pointed to by Y. Y is unchanged.

STORE-VIA-X-AUTOINCREMENT—Pop the top item of the Parameter Stack and store it in the memory location pointed to by X. After storing, increment the most significant 30 bits of X to point to the next 32-bit word address.

STORE-VIA-Y-AUTOINCREMENT—Pop the top item of the Parameter Stack and store it in the memory location pointed to by Y. After storing, increment the most significant 30 bits of Y to point to the next 32-bit word address.

STORE-VIA-X-AUTODECREMENT—Pop the top item of the Parameter Stack and store it in the memory location pointed to by X. After storing, decrement the most significant 30 bits of X to point to the previous 32-bit word address.

STORE-VIA-Y-AUTODECREMENT—Pop the top item of the Parameter Stack and store it in the memory location pointed to by Y. After storing, decrement the most significant 30 bits of Y to point to the previous 32-bit word address.

FEICH-VIA-PC—Fetch the 32-bit memory content pointed to by the Program Counter and push it onto the Parameter Stack. After fetching, increment the most significant 30 bits of the Program Counter to point to the next 32-bit word address.

*NOTE: When this instruction executes, the PC is pointing to the memory location following the instruction. The effect

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is of loading a 32-bit immediate operand. This is an 8-bit instruction and therefore will be combined with other 8-bit instructions in a 4-byte instruction fetch. It is possible to have from one to four FETCH-VIA-PC instructions in a 4-byte instruction fetch. The PC increments after each execution of FETCH-VIA-PC, so it is possible to push four immediate operands on the stack. The four operands would be the found in the four memory locations following the instruction.

BYTE-FETCH-VIA-X—Fetch the 32-bit memory content pointed to by the most significant 30 bits of X. Using the two least significant bits of X, select one of four bytes from the 32-bit memory fetch, right justify the byte in a 32-bit field and push the selected byte preceded by leading zeros onto the Parameter Stack.

BYTE-STORE-VIA-X—Fetch the 32-bit memory content pointed to by the most significant 30 bits of X. Pop the TOP item from the Parameter Stack. Using the two least significant bits of X place the least significant byte into the 32-bit memory data and write the 32-bit entity back to the location pointed to by the most significant 30 bits of X.

OTHER EFFECTS OF MEMORY ACCESS INSTRUCTIONS:

Any FETCH instruction will push a value on the Parameter Stack 74. If the on-chip stack is full, the stack will overflow into off-chip memory stack resulting in an additional memory cycle. Any STORE instruction will pop a value from the Parameter Stack 74. If the on-chip stack is empty, a memory cycle will be generated to fetch a value from off-chip memory stack.

HANDLING ON-CHIP VARIABLES

High-level languages often allow the creation of LOCAL VARIABLES. These variables are used by a particular procedure and discarded. In cases of nested procedures, layers of these variables must be maintained. On-chip storage is up to five times faster than off-chip RAM, so a means of keeping local variables on-chip can make operations run faster. The microprocessor 50 provides the capability for both on-chip storage of local variables and nesting of multiple levels of variables through the Return Stack.

The Return Stack 134 is implemented as 16 on-chip RAM locations. The most common use for the Return Stack 134 is storage of return addresses from subroutines and interrupt calls. The microprocessor allows these 16 locations to also be used as addressable registers. The 16 locations may be read and written by two instructions which indicate a Return Stack relative address from 0-15. When high-level procedures are nested, the current procedure variables push the previous procedure variables further down the Return Stack 134. Eventually, the Return Stack will automatically overflow into off-chip RAM.

ON-CHIP VARIABLE INSTRUCTIONS

READ-LOCAL-VARIABLE XXXX—Read the XXXXth location relative to the top of the Return Stack (XXXX is a binary number from 0000-1111). Push the item read onto the Parameter Stack. **OTHER EFFECTS:** If the Parameter Stack is full, the push operation will cause a memory cycle to be generated as one item of the stack is automatically stored to external RAM. The logic which selects the location performs a modulo 16 subtraction. If four local variables have been pushed onto the Return Stack, and an instruction attempts to READ the fifth item, unknown data will be returned.

WRITE-LOCAL-VARIABLE XXXX—Pop the TOP item of the Parameter Stack and write it into the

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XXXXth location relative to the top of the Return Stack (XXXX is a binary number from 0000-1111). **OTHER EFFECTS:** If the Parameter Stack is empty, the pop operation will cause a memory cycle to be generated to fetch the Parameter Stack item 30 from external RAM. The logic which selects the location performs a modulo 16 subtraction. If four local variables have been pushed onto the Return Stack, and an instruction attempts to WRITE to the fifth item, it is possible to clobber return addresses or wreak other havoc.

REGISTER AND FLIP-FLOP TRANSFER AND PUSH INSTRUCTIONS

DROP—Pop the TOP item from the Parameter Stack and discard it.

SWAP—Exchange the data in the TOP Parameter Stack location with the data in the NEXT Parameter Stack location.

DUP—Duplicate the TOP item on the Parameter Stack and push it onto the Parameter Stack.

PUSH-LOOP-COUNTER—Push the value in LOOP COUNTER onto the Parameter Stack.

POP-RSTACK-PUSH-TO-STACK—Pop the top item from the Return Stack and push it onto the Parameter Stack.

PUSH-X-REG—Push the value in the X Register onto the Parameter Stack.

PUSH-STACK-POINTER—Push the value of the Parameter Stack pointer onto the Parameter Stack.

PUSH-RSTACK-POINTER—Push the value of the Return Stack pointer onto the Return Stack.

PUSH-MODE-BITS—Push the value of the MODE REGISTER onto the Parameter Stack.

PUSH-INPUT—Read the 10 dedicated input bits and push the value (right justified and padded with leading zeros) onto the Parameter Stack.

SET-LOOP-COUNTER—Pop the TOP value from the Parameter Stack and store it into LOOP COUNTER.

POP-STACK-PUSH-TO-RSTACK—Pop the TOP item from the Parameter Stack and push it onto the Return Stack.

SET-X-REG—Pop the TOP item from the Parameter Stack and store it into the X Register.

SET-STACK-POINTER—Pop the TOP item from the Parameter Stack and store it into the Stack Pointer.

SET-RSTACK-POINTER—Pop the TOP item from the Parameter Stack and store it into the Return Stack Pointer.

SET-MODE-BITS—Pop the TOP value from the Parameter Stack and store it into the MODE BITS.

SET-OUTPUT—Pop the TOP item from the Parameter Stack and output it to the 10 dedicated output bits. **OTHER EFFECTS:** Instructions which push or pop the Parameter Stack or Return Stack may cause a memory cycle as the stacks overflow back and forth between on-chip and off-chip memory.

LOADING A SHORT LITERAL

A special case of register transfer instruction is used to push an 8-bit literal onto the Parameter Stack. This instruction requires that the 8-bits to be pushed reside in the last byte of a 4-byte instruction group. The instruction op-code loading the literal may reside in ANY of the other three bytes in the instruction group.

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EXAMPLE

BYTE 1	BYTE 2	BYTE 3
LOAD-SHORT-LITERAL	QQQQQQQQ	QQQQQQQQ
BYTE 4		
00001111		

In this example, QQQQQQQQ indicates any other 8-bit instruction. When Byte 1 is executed, binary 00001111 (HEX 0F) from Byte 4 will be pushed (right justified and padded by leading zeros) onto the Parameter Stack. Then the instructions in Byte 2 and Byte 3 will execute. The micro-processor instruction decoder knows not to execute Byte 4. It is possible to push three identical 8-bit values as follows:

BYTE 1	BYTE 2
LOAD-SHORT-LITERAL	LOAD-SHORT-LITERAL
BYTE 3	BYTE 4
LOAD-SHORT-LITERAL	00001111

SHORT-LITERAL-INSTRUCTION

LOAD-SHORT-LITERAL—Push the 8-bit value found in Byte 4 of the current 4-byte instruction group onto the Parameter Stack.

LOGIC INSTRUCTIONS

Logical and math operations use the stack for the source of one or two operands and as the destination for results. The stack organization is a particularly convenient arrangement for evaluating expressions. TOP indicates the top value on the Parameter Stack. 74 NEXT indicates the next to top value on the Parameter Stack. 74

AND—Pop TOP and NEXT from the Parameter Stack, perform the logical AND operation on these two operands, and push the result onto the Parameter Stack.

OR—Pop TOP and NEXT from the Parameter Stack, perform the logical OR operation on these two operands, and push the result onto the Parameter Stack.

XOR—Pop TOP and NEXT from the Parameter Stack, perform the logical exclusive OR on these two operands, and push the result onto the Parameter Stack.

BIT-CLEAR—Pop TOP and NEXT from the Parameter Stack, toggle all bits in NEXT, perform the logical AND operation on TOP, and push the result onto the Parameter Stack. (Another way of understanding this instruction is thinking of it as clearing all bits in TOP that are set in NEXT.)

MATH INSTRUCTIONS

Math instruction pop the TOP item and NEXT to top item of the Parameter Stack 74 to use as the operands. The results are pushed back on the Parameter Stack. The CARRY flag is used to latch the "33rd bit" of the ALU result.

ADD—Pop the TOP item and NEXT to top item from the Parameter Stack, add the values together and push the result back on the Parameter Stack. The CARRY flag may be changed.

ADD-WITH-CARRY—Pop the TOP item and the NEXT to top item from the Parameter Stack, add the values together. If the CARRY flag is "1" increment the result. Push the ultimate result back on the Parameter Stack. The CARRY flag may be changed.

ADD-X—Pop the TOP item from the Parameter Stack and read the third item from the top of the Parameter

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Stack. Add the values together and push the result back on the Parameter Stack. The CARRY flag may be changed.

SUB—Pop the TOP item and NEXT to top item from the Parameter Stack, Subtract NEXT from TOP and push the result back on the Parameter Stack. The CARRY flag may be changed.

SUB-WITH-CARRY—Pop the TOP item and NEXT to top item from the Parameter Stack. Subtract NEXT from TOP. If the CARRY flag is "1" increment the result. Push the ultimate result back on the Parameter Stack. The CARRY flag may be changed.

SUB-X—

SIGNED-MULT-STEP—

UNSIGNED-MULT-STEP—

SIGNED-FAST-MULT—

FAST-MULT-STEP—

UNSIGNED-DIV-STEP—

GENERATE-POLYNOMIAL—

ROUND—

COMPARE—Pop the TOP item and NEXT to top item from the Parameter Stack. Subtract NEXT from TOP. If the result has the most significant bit equal to "0" (the result is positive), push the result onto the Parameter Stack. If the result has the most significant bit equal to "1" (the result is negative), push the old value of TOP onto the Parameter Stack. The CARRY flag may be affected.

SHIFT/ROTATE

SHIFT-LEFT—Shift the TOP Parameter Stack item left one bit. The CARRY flag is shifted into the least significant bit of TOP.

SHIFT-RIGHT—Shift the TOP Parameter Stack item right one bit. The least significant bit of TOP is shifted into the CARRY flag. Zero is shifted into the most significant bit of TOP.

DOUBLE-SHIFT-LEFT—Treating the TOP item of the Parameter Stack as the most significant word of a 64-bit number and the NEXT stack item as the least significant word, shift the combined 64-bit entity left one bit. The CARRY flag is shifted into the least significant bit of NEXT.

DOUBLE-SHIFT-RIGHT—Treating the TOP item of the Parameter Stack as the most significant word of a 64-bit number and the NEXT stack item as the least significant word, shift the combined 64-bit entity right one bit. The least significant bit of NEXT is shifted into the CARRY flag. Zero is shifted into the most significant bit of TOP.

OTHER INSTRUCTIONS

FLUSH-STACK—Empty all on-chip Parameter Stack locations into off-chip RAM. (This instruction is useful for multitasking applications.) This instruction accesses a counter which holds the depth of the on-chip stack and can require from none to 16 external memory cycles.

FLUSH-RSTACK—Empty all on-chip Return Stack locations into off-chip RAM. (This instruction is useful for multitasking applications.) This instruction accesses a counter which holds the depth of the on-chip Return Stack and can require from none to 16 external memory cycles.

It should further be apparent to those skilled in the art that various changes in form and details of the invention as

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shown and described may be made. It is intended that such changes be included within the spirit and scope of the claims appended hereto

What is claimed is:

1 A microprocessor integrated circuit comprising:

a program-controlled processing unit operative in accordance with a sequence of program instructions;

a memory coupled to said processing unit and capable of storing information provided by said processing unit;

a plurality of column latches coupled to the processing unit and the memory, wherein, during a read operation, a row of bits are read from the memory and stored in the column latch; and

a variable speed system clock having an output coupled to said processing unit;

said processing unit, said variable speed system clock, said plurality of column latches, and said memory fabricated on a single substrate, said memory using a greater area of said single substrate than said processing unit, said memory further using a majority of a total area of said single substrate

2 The microprocessor integrated circuit of claim 1 wherein said memory is dynamic random-access memory.

3 The microprocessor integrated circuit of claim 1 wherein said memory is static random-access memory

4 A microprocessor integrated circuit comprising:

a processing unit disposed upon an integrated circuit substrate, said processing unit operating in accordance with a predefined sequence of program instructions;

a memory coupled to said processing unit and capable of storing information provided by said processing unit, said memory occupying a larger area of said integrated circuit substrate than said processing unit said memory further occupying a majority of a total area of said single substrate; and

a ring oscillator having a variable output frequency, wherein the ring oscillator provides a system clock to the processing unit, the ring oscillator disposed on said integrated circuit substrate.

5 The microprocessor integrated circuit of claim 4 wherein said memory is dynamic random-access memory

6 The microprocessor integrated circuit of claim 4 wherein said memory is static random-access memory

7 The microprocessor integrated circuit of claim 4 wherein said memory is capable of supporting read and write operations

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8 A microprocessor integrated circuit comprising:

a processing unit having one or more interface ports for interprocessor communication, said processing unit being disposed on a single substrate;

a memory disposed upon said substrate and coupled to said processing unit, said memory occupying a greater area of said substrate than said processing unit, said memory further comprising a majority of a total area of said substrate; and

a ring oscillator having a variable output frequency, wherein the ring oscillator provides a system clock to the processing unit, the ring oscillator disposed on said substrate

9 The microprocessor integrated circuit of claim 8 wherein a first of said interface ports includes a column latch, said column latch facilitating serial communication through said first of said interface ports

10 The microprocessor integrated circuit of claim 8 further including memory controller means coupled to said memory for performing direct memory access data transfer through said one or more interface ports

11 A microprocessor computational system comprising:

a first processing unit disposed upon a first substrate;

a first memory disposed upon said first substrate and coupled to said first processing unit, said first memory occupying a greater area of said first substrate than said first processing unit, said memory further occupying a majority of a total area of said substrate;

a ring oscillator having a variable output frequency, wherein the ring oscillator provides a system clock to the processing unit, the ring oscillator disposed on said first substrate; and

a second processing unit coupled to said first processing unit and configured for interprocessor communication with said first processing unit

12 The microprocessor computational system of claim 11 wherein said second processing unit and a second memory are disposed upon a second substrate, said second memory occupying a greater area of said second substrate than said second processing unit said second memory further occupying a majority of a total area of said substrate

13 The multiprocessor computational system of claim 11 wherein said first processing unit includes an interface port for establishing said interprocessor communication between an internal register of said first processing unit and second processing unit

* * * * *

EXHIBIT B



US005,336A

United States Patent [19]

Moore et al.

[11] Patent Number: **5,809,336**[45] Date of Patent: **Sep. 15, 1998**

[54] **HIGH PERFORMANCE MICROPROCESSOR
HAVING VARIABLE SPEED SYSTEM
CLOCK**

[75] Inventors: Charles H. Moore, Woodside; Russell
H. Fish, III, Mt View, both of Calif

[73] Assignee: Patriot Scientific Corporation, San
Diego, Calif

[21] Appl No: 484,918

[22] Filed: Inn. 7, 1995

Related U.S. Application Data

[62] Division of Ser. No. 389 334, Aug 3, 1989, Pat No
5,440,749

[51] Int. Cl.⁶ G06F 1/04

[52] U.S. Cl. 395/845

[58] Field of Search 395/500, 551,
395/555, 845

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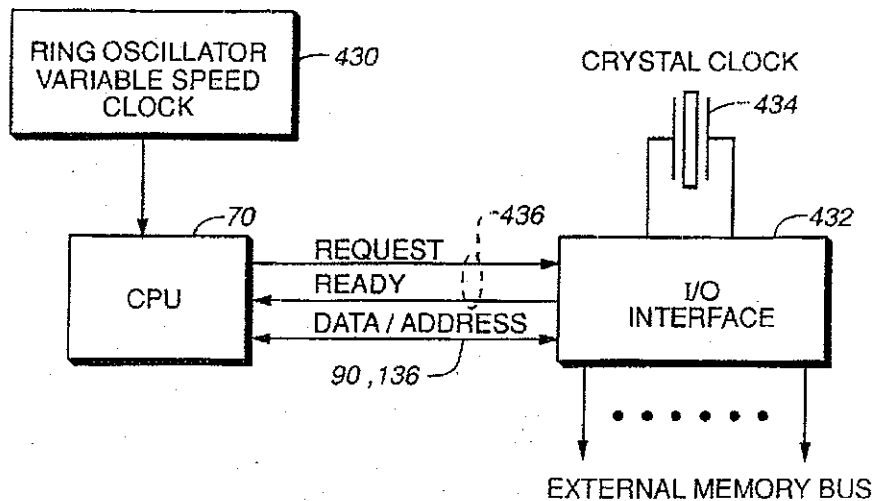
Primary Examiner—David Y Eng

Attorney, Agent, or Firm—Cooley Godward LLP

[57] **ABSTRACT**

A high performance, low cost microprocessor system having a variable speed system clock is disclosed herein. The microprocessor system includes an integrated circuit having a central processing unit and a ring oscillator variable speed system clock for clocking the microprocessor. The central processing unit and ring oscillator variable speed system clock each include a plurality of electronic devices of like type which allows the central processing unit to operate at a variable processing frequency dependent upon a variable speed of the ring oscillator variable speed system clock. The microprocessor system may also include an input/output interface connected to exchange coupling control signals, address and data with the central processing unit. The input/output interface is independently clocked by a second clock connected thereto.

10 Claims, 19 Drawing Sheets



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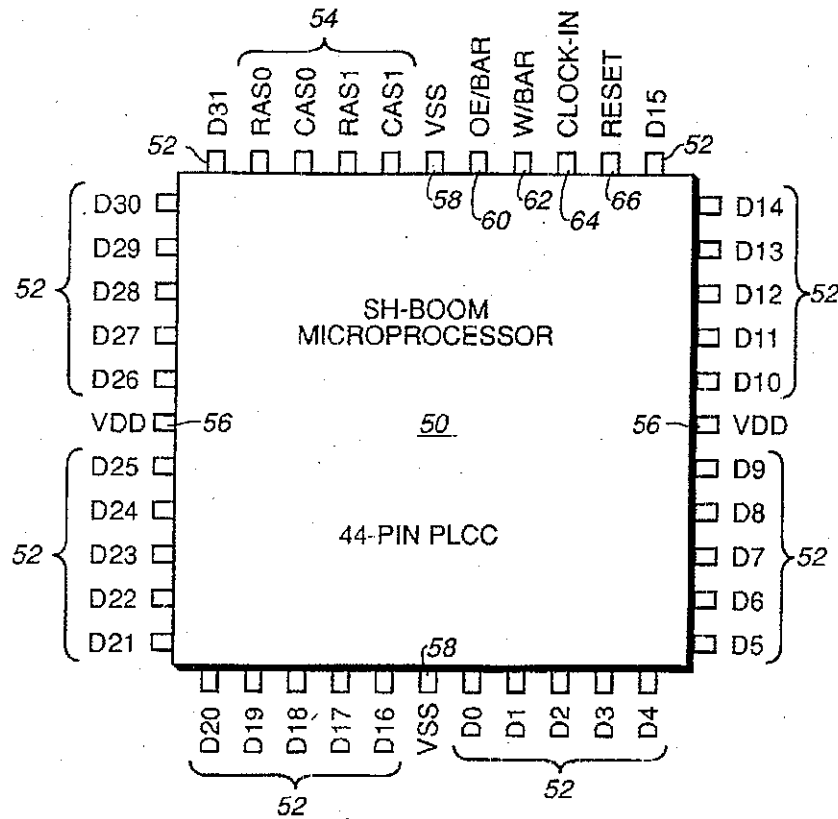


FIG. 1

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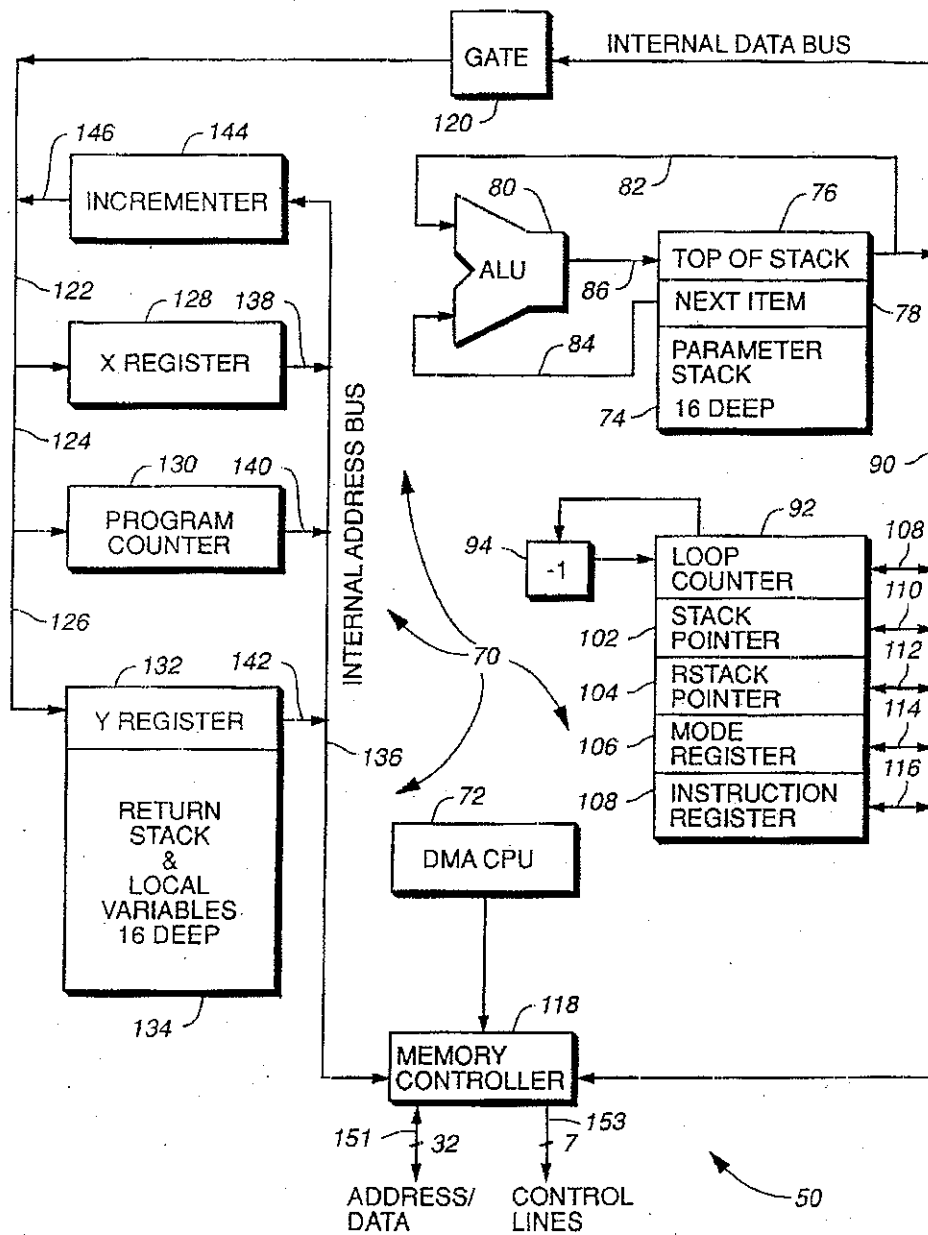


FIG. 2

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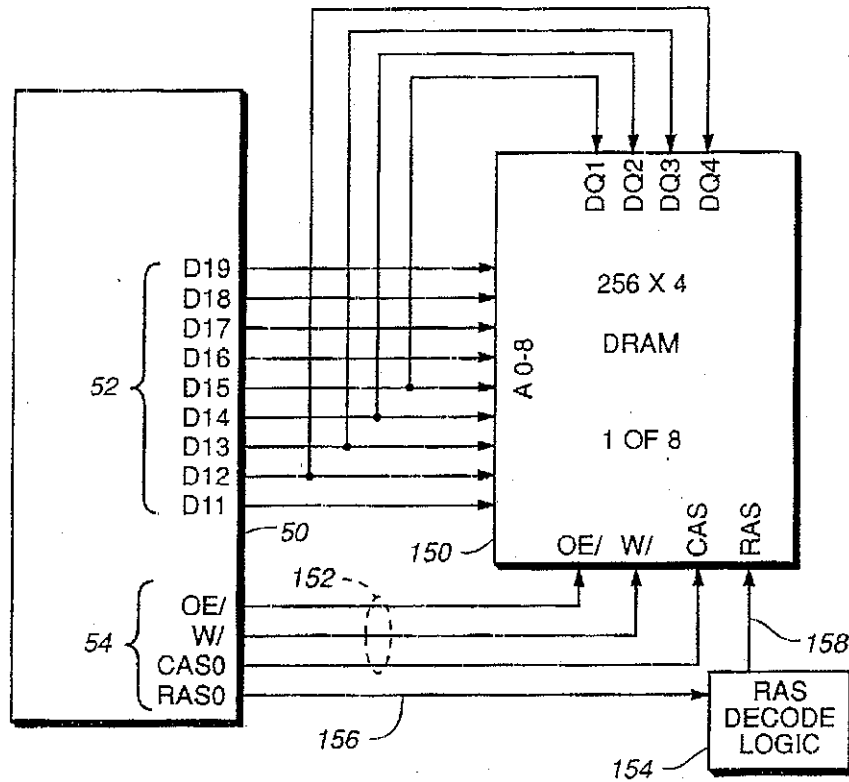


FIG. 3

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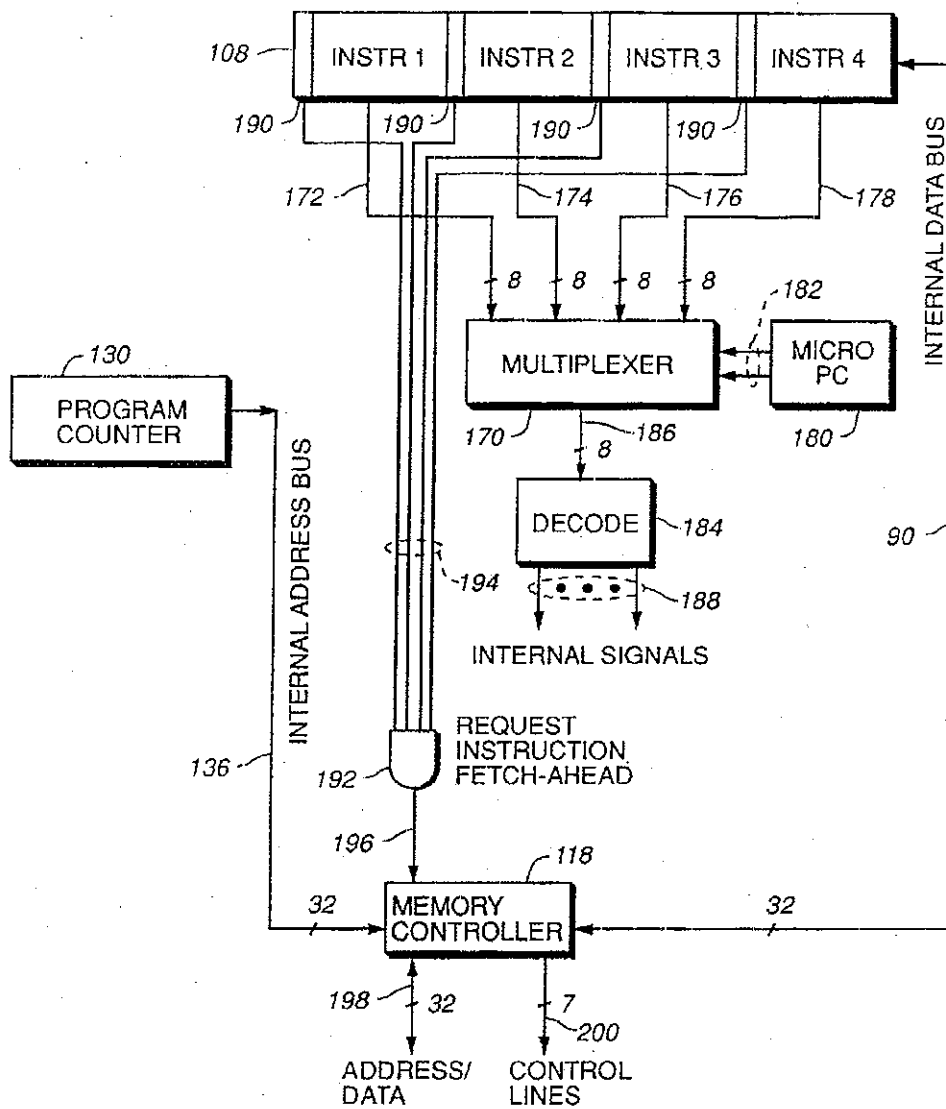


FIG. 4

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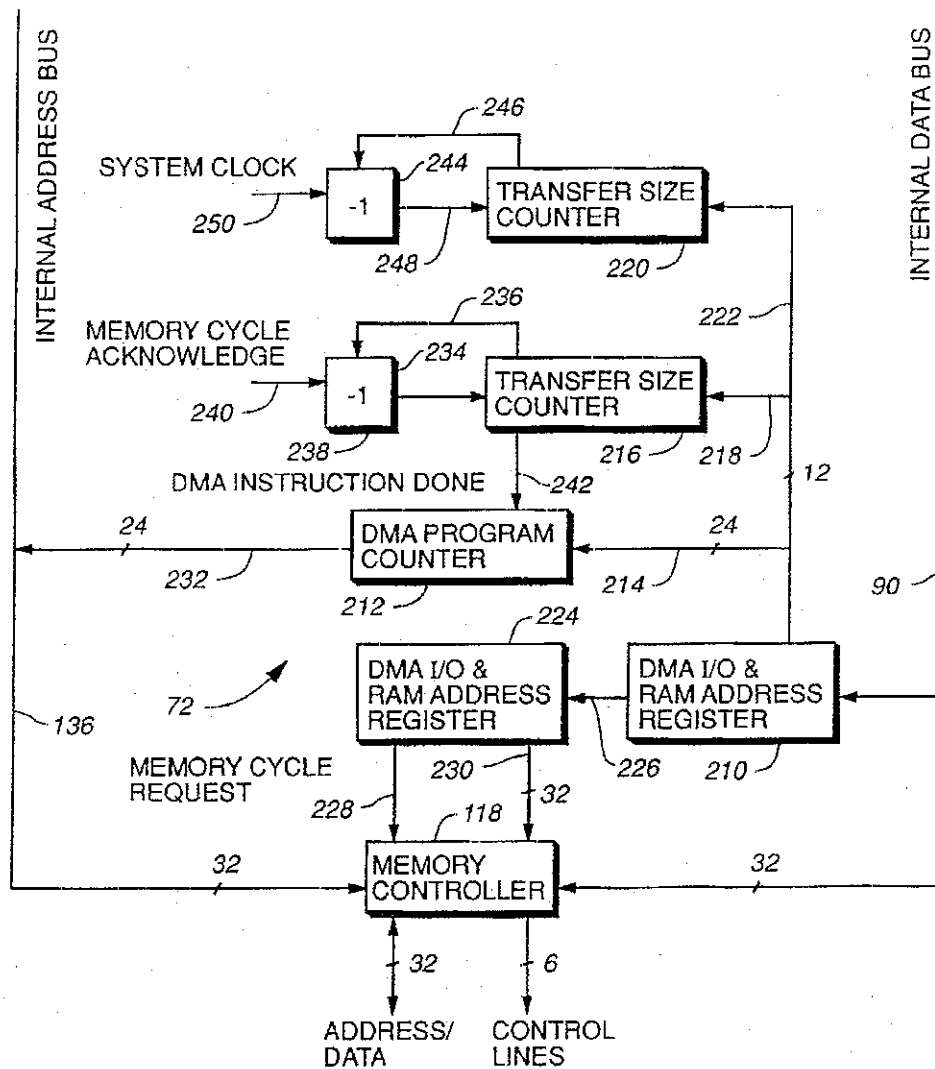


FIG. 5

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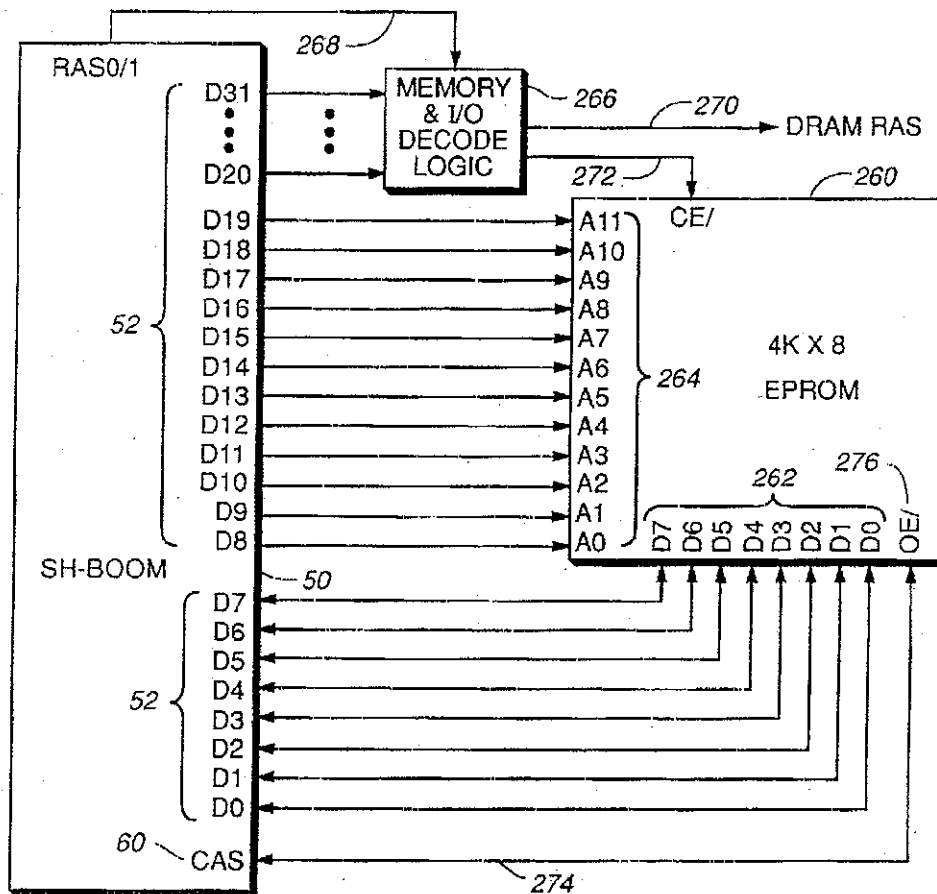


FIG. 6

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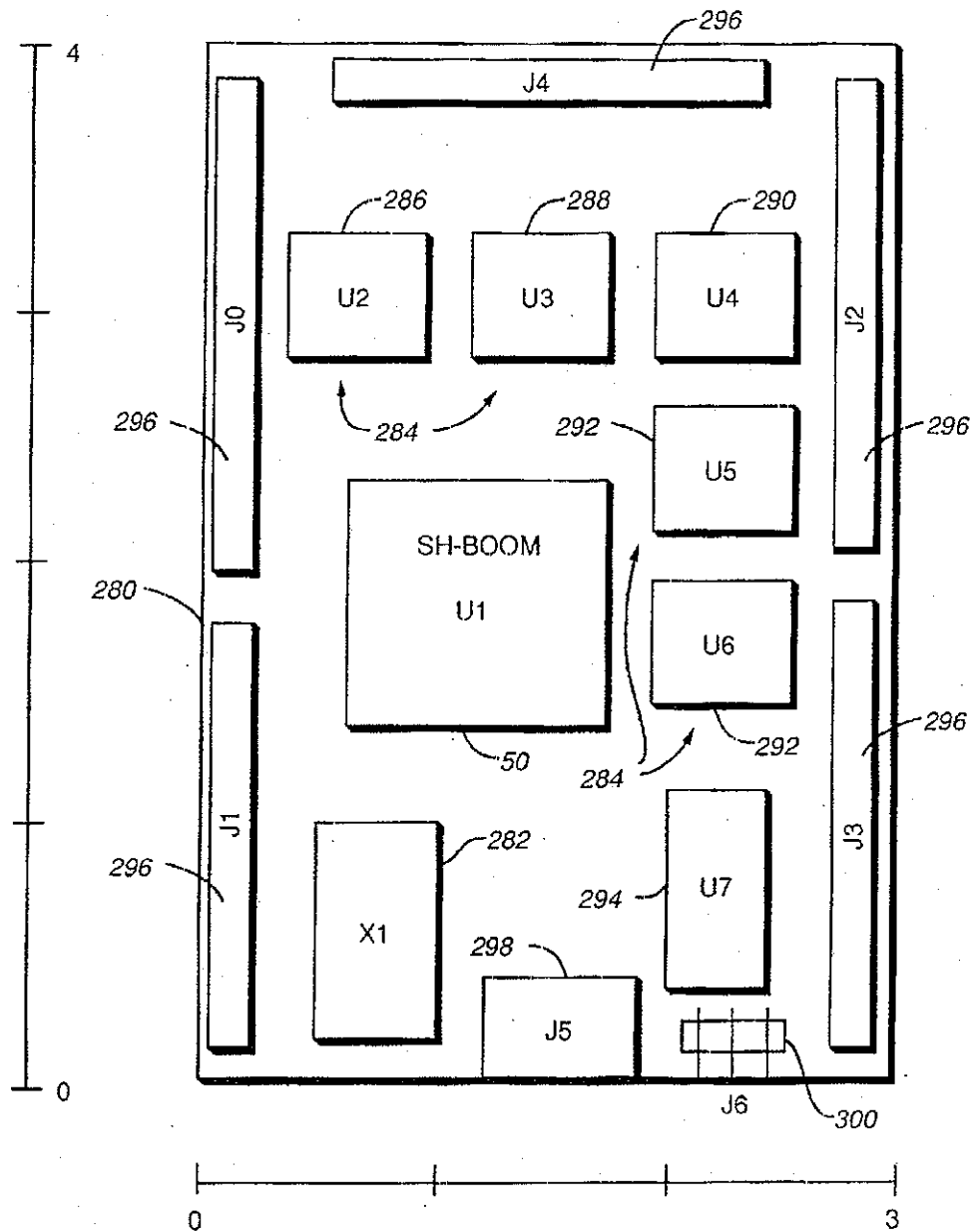


FIG. 7

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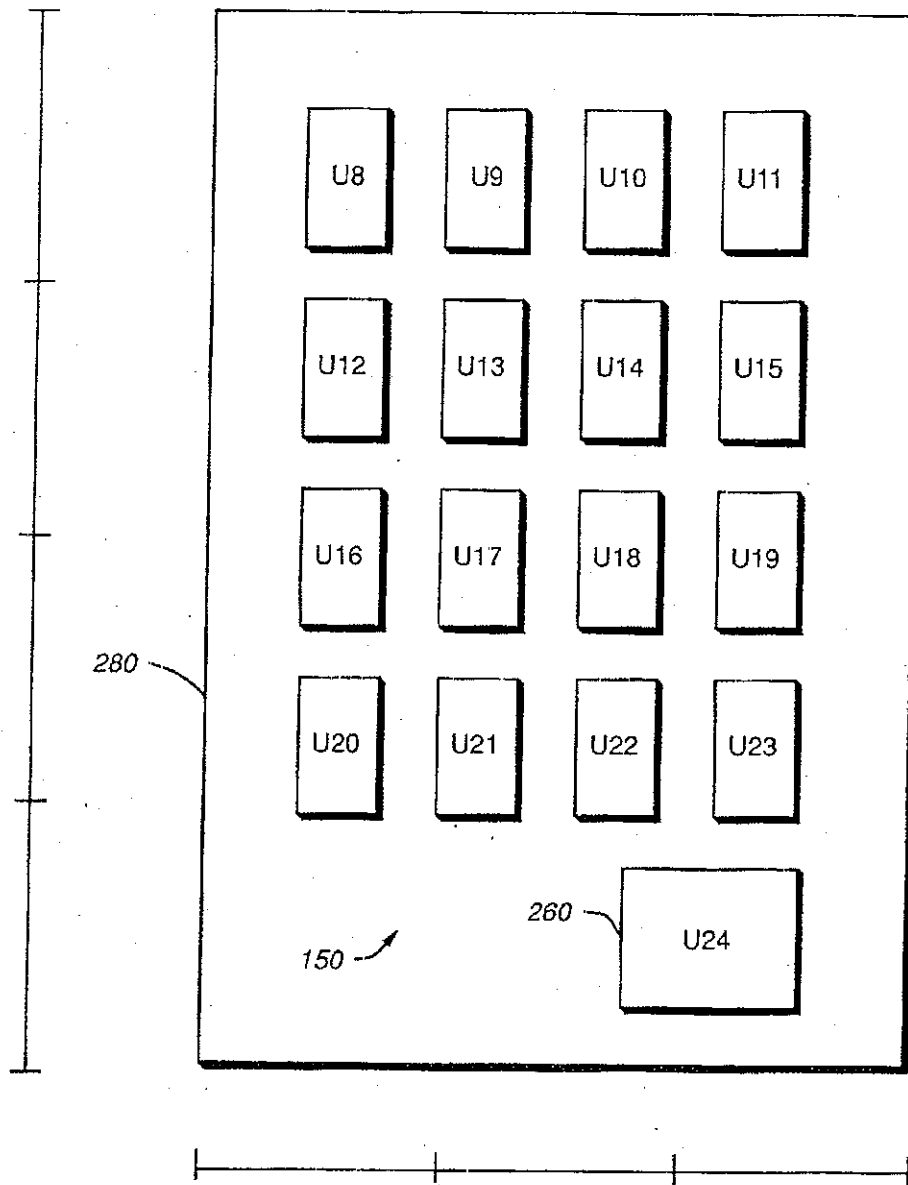


FIG. 8

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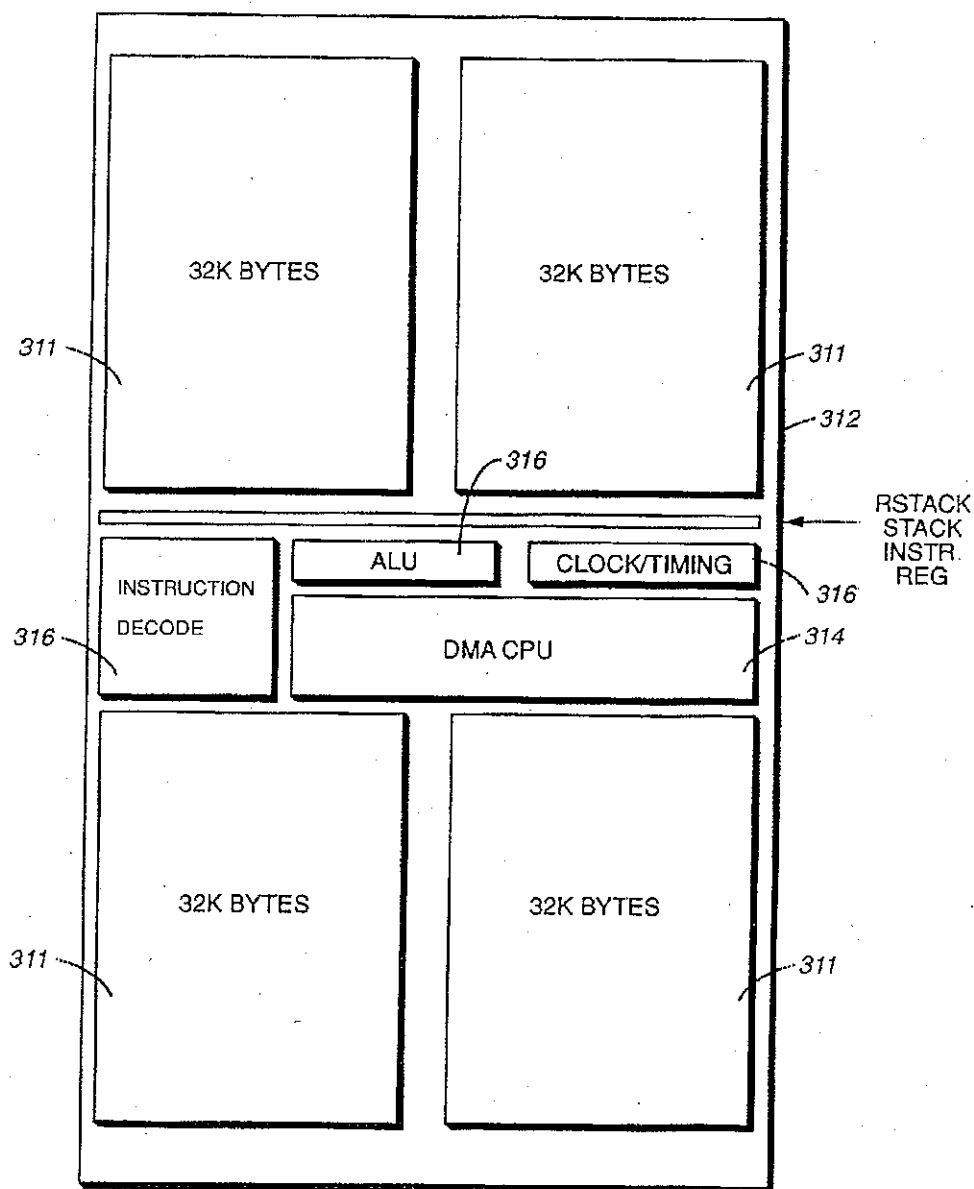


FIG. 9

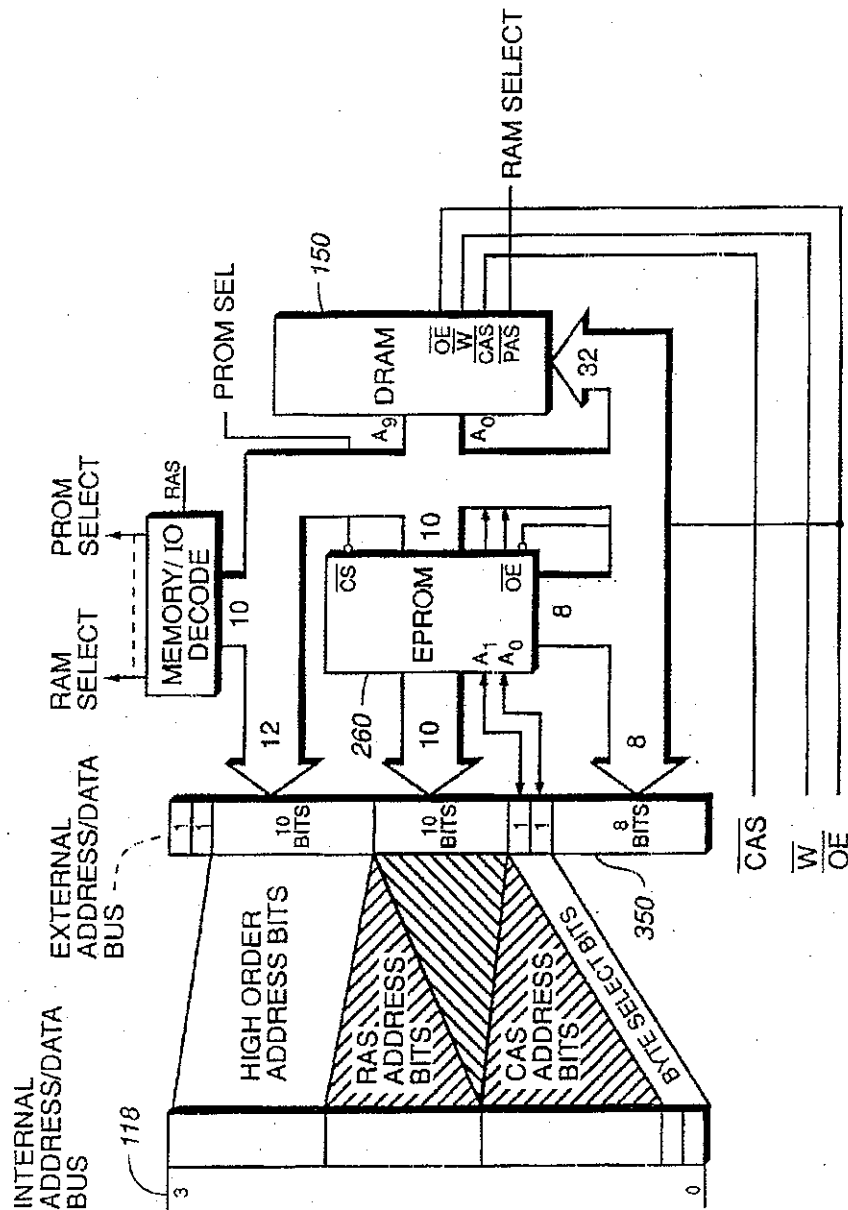


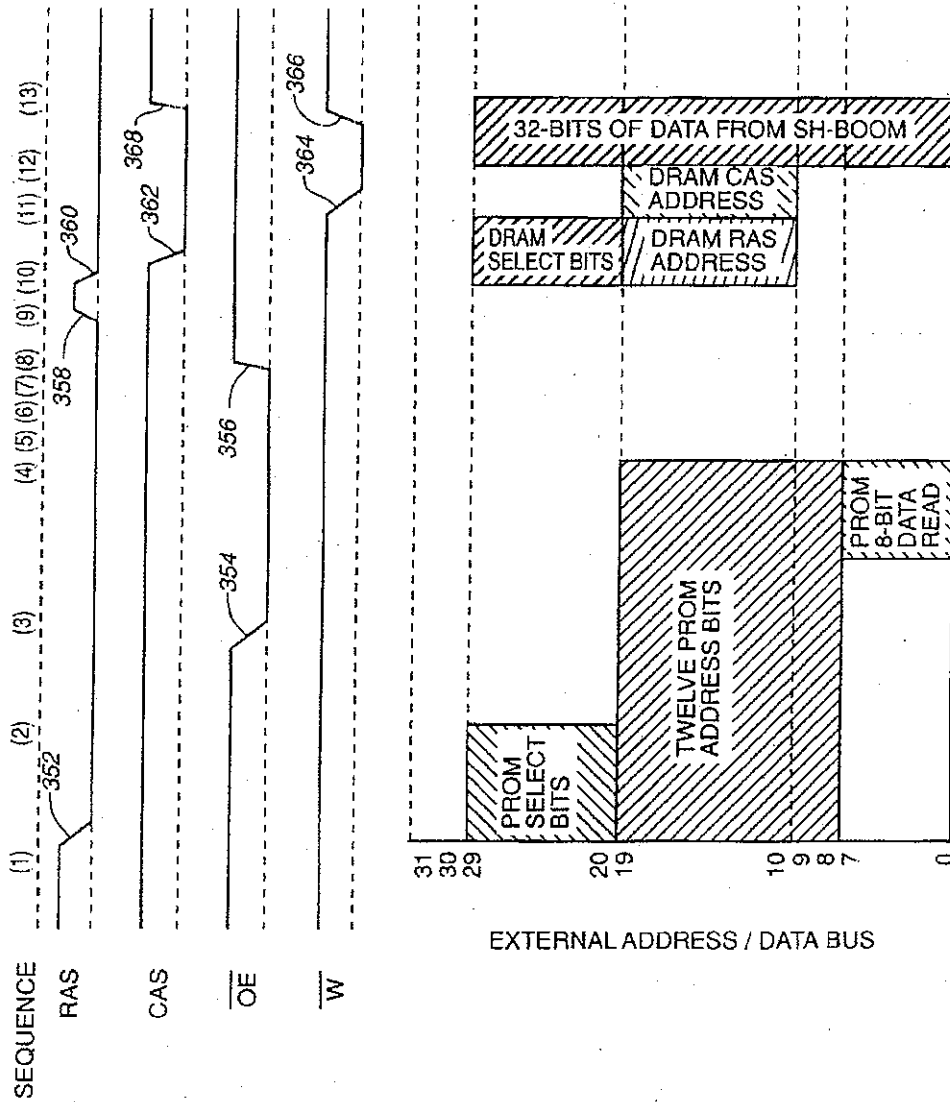
FIG. 10

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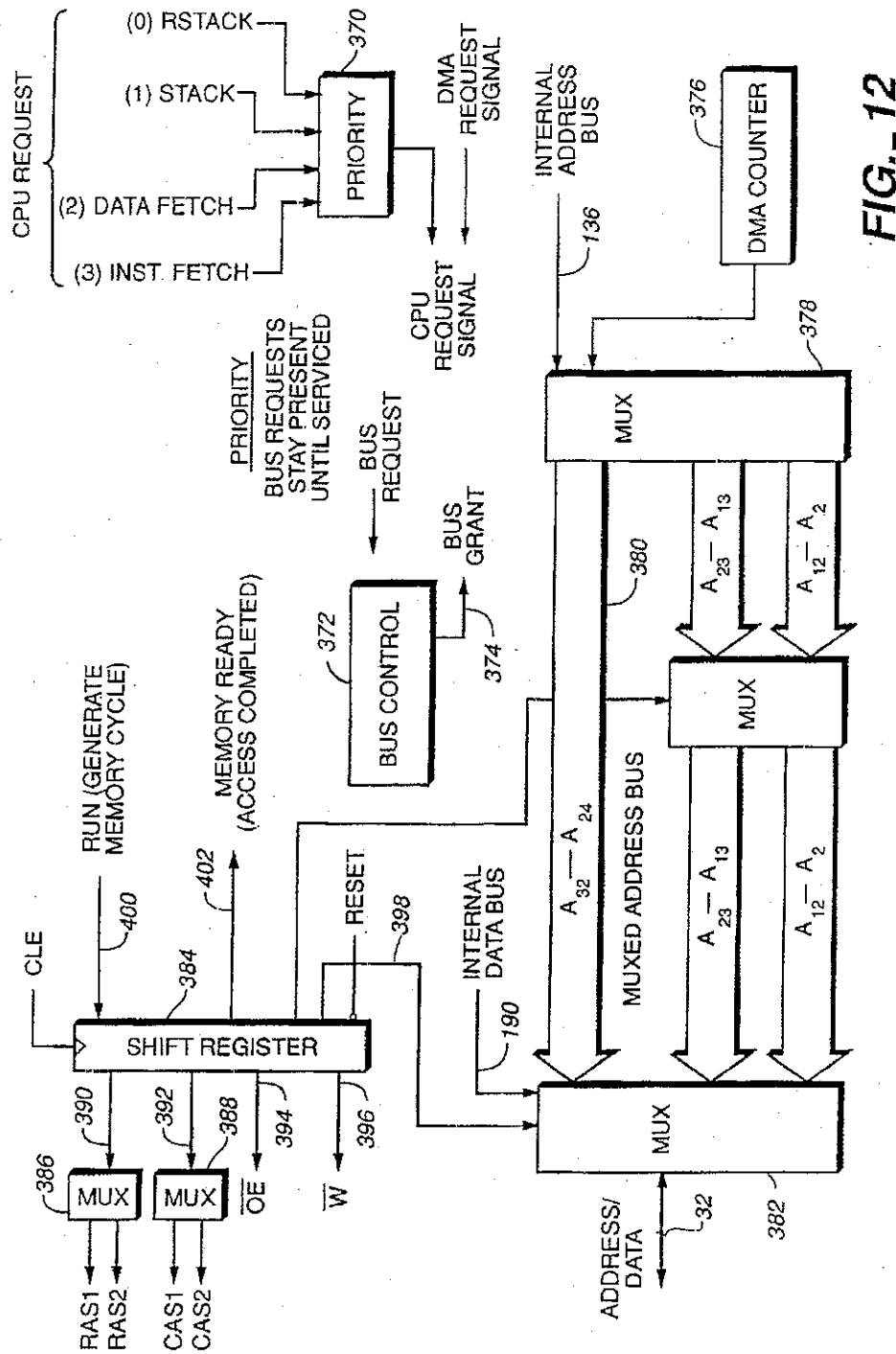


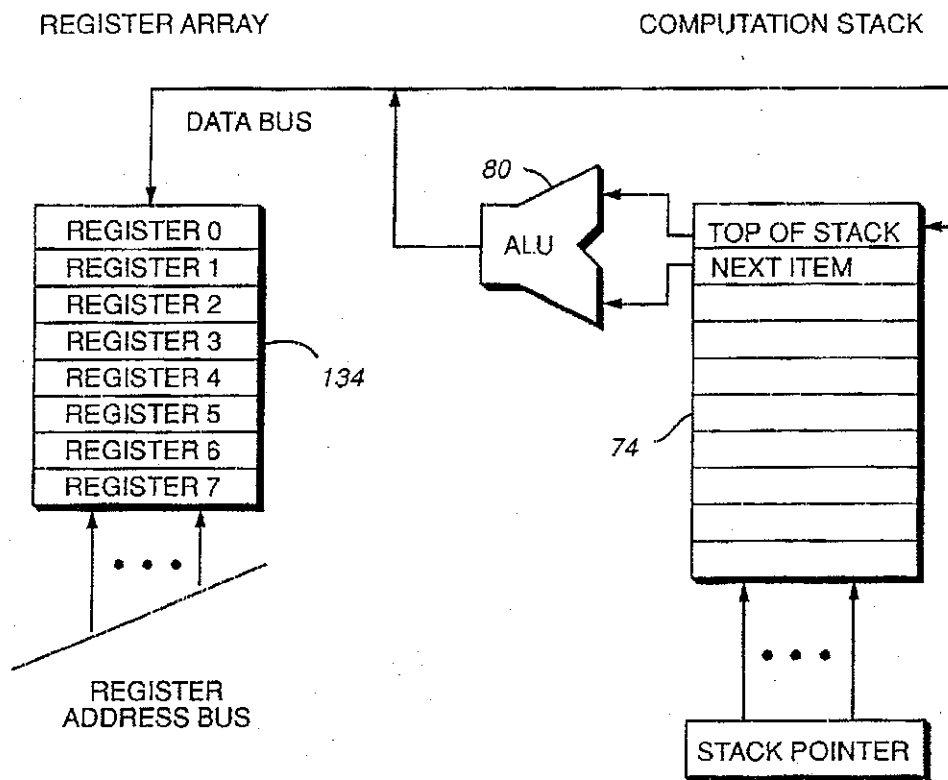
FIG. 12

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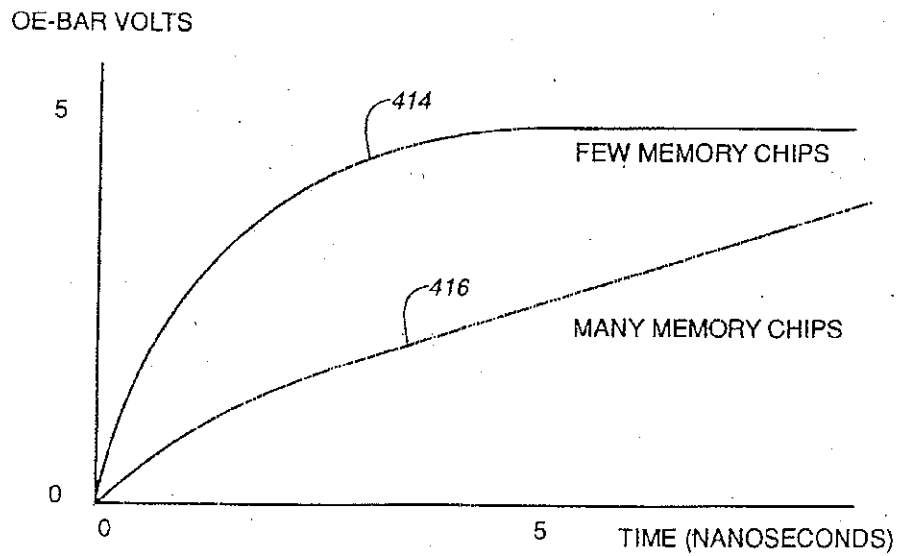
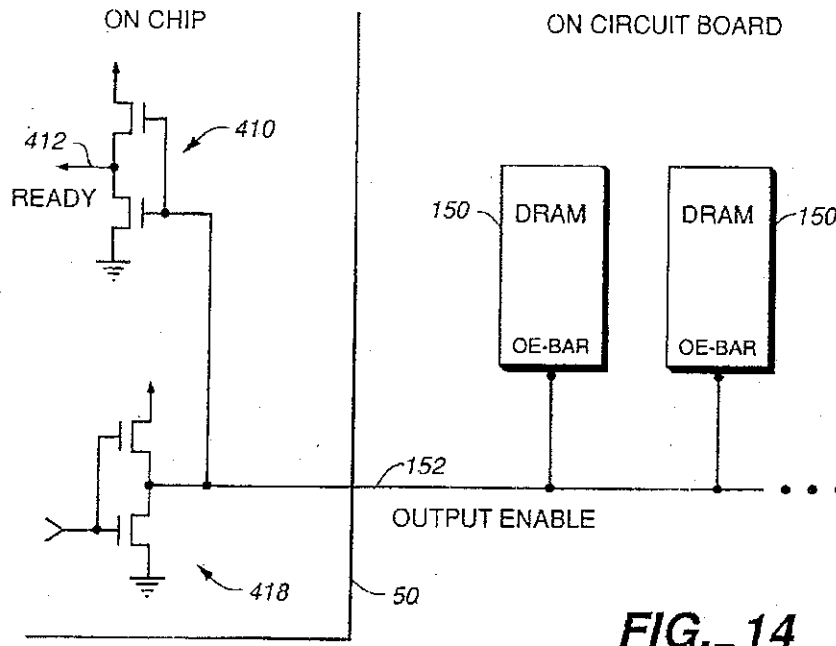
**FIG. 13**

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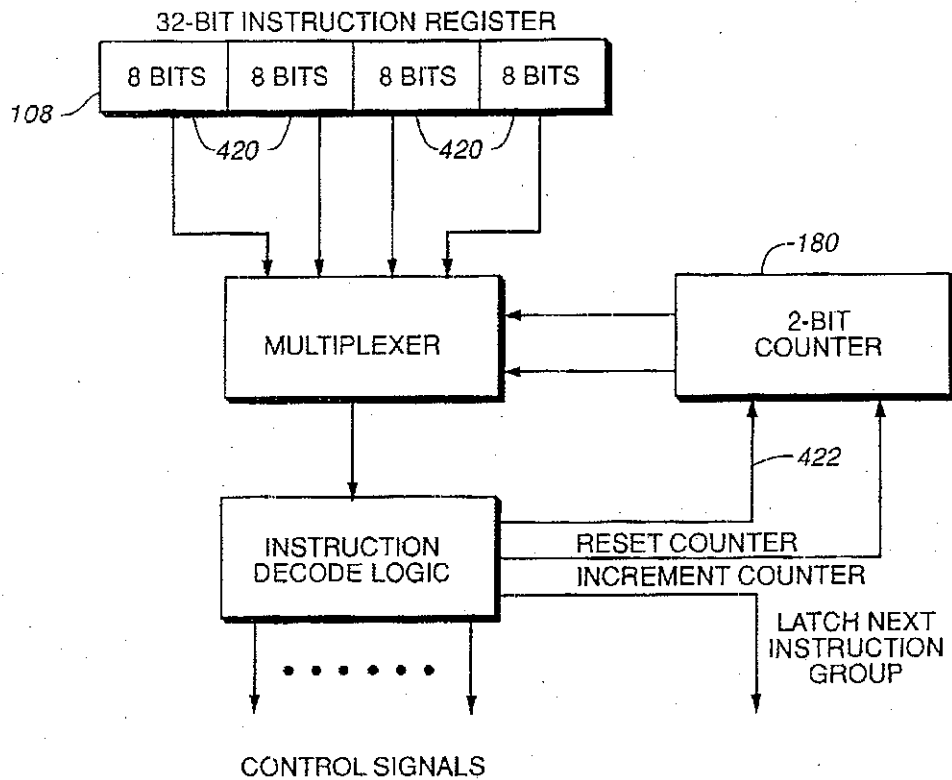
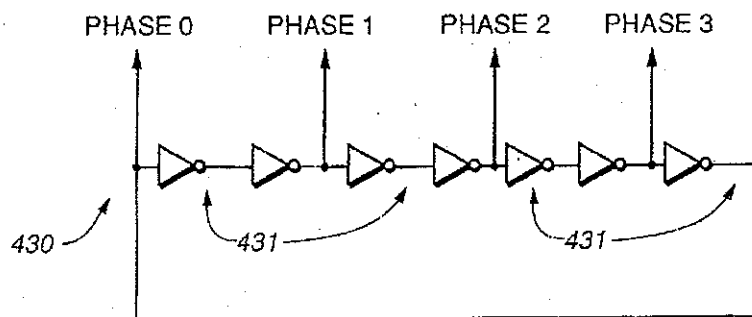


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**FIG. 16****FIG. 18**

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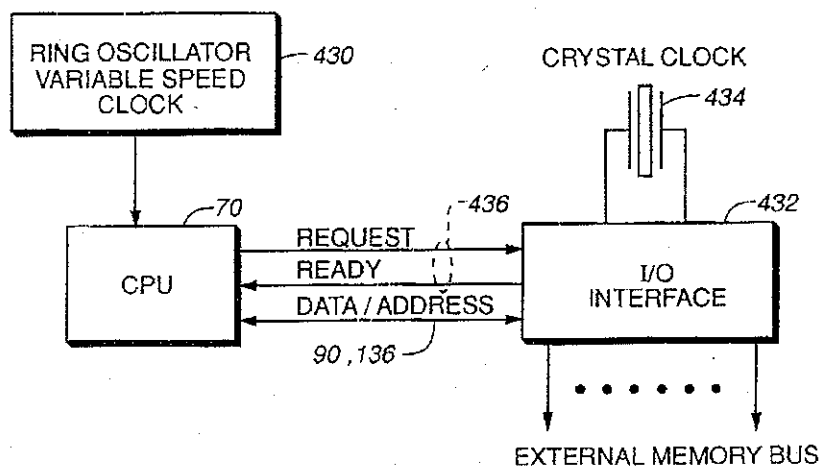


FIG. 17

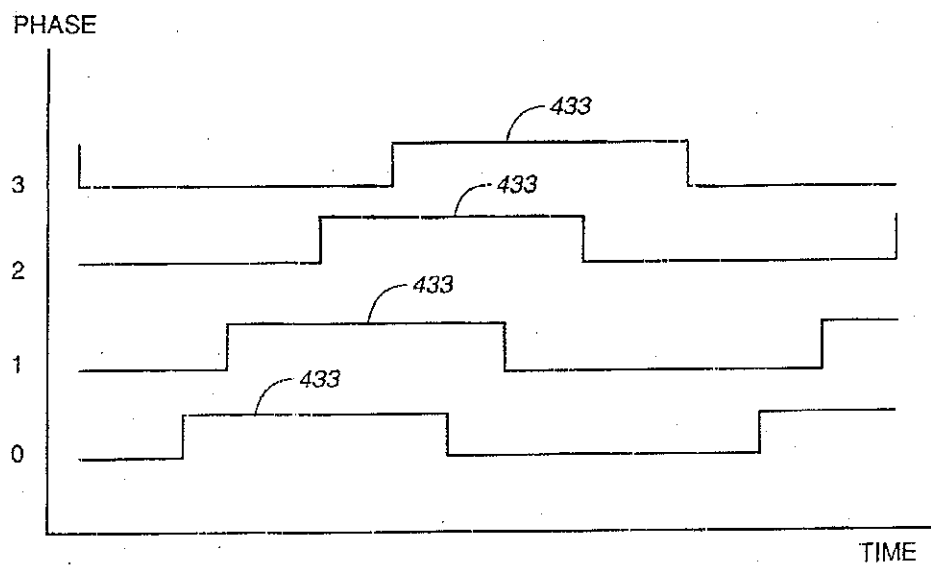


FIG. 19

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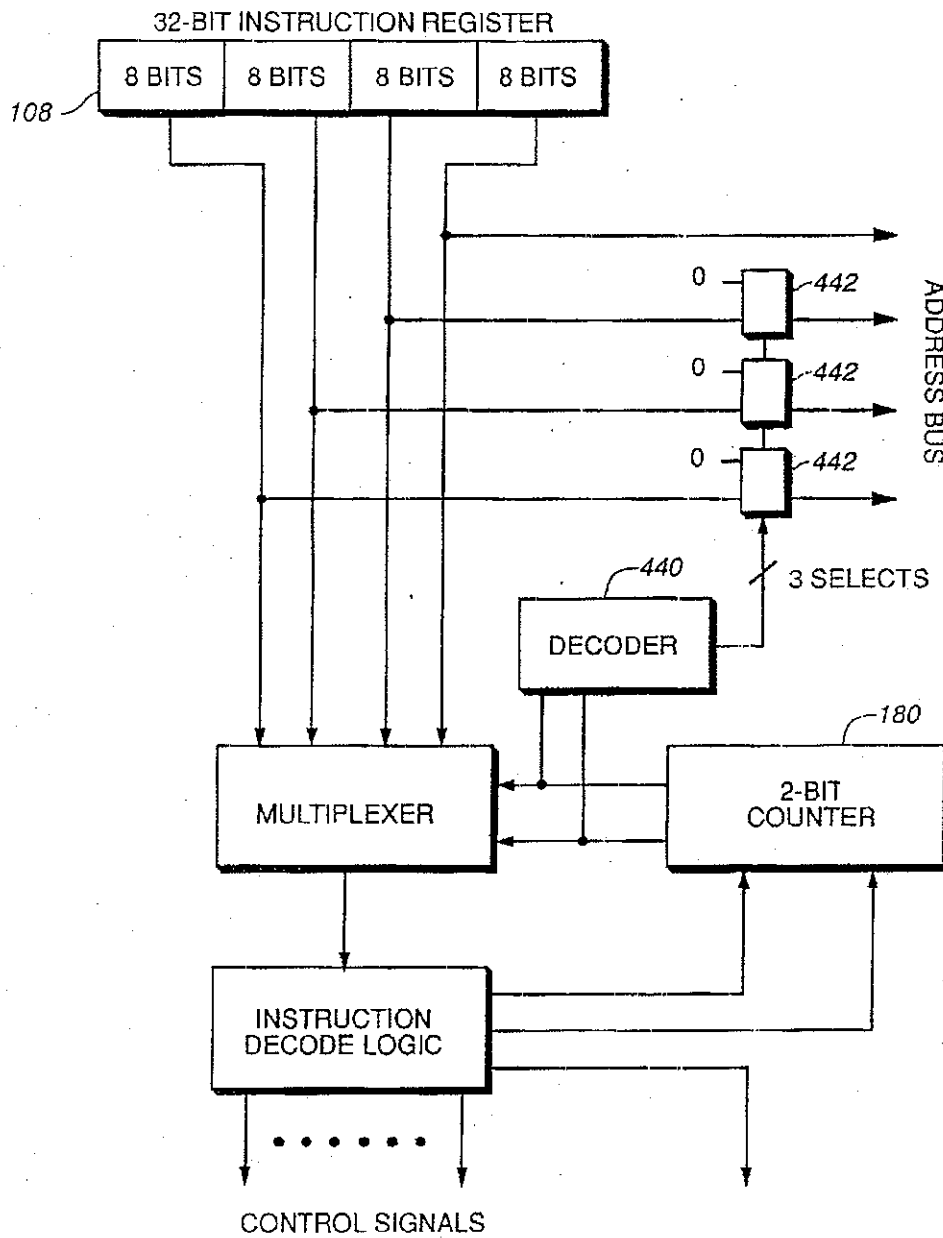


FIG. 20

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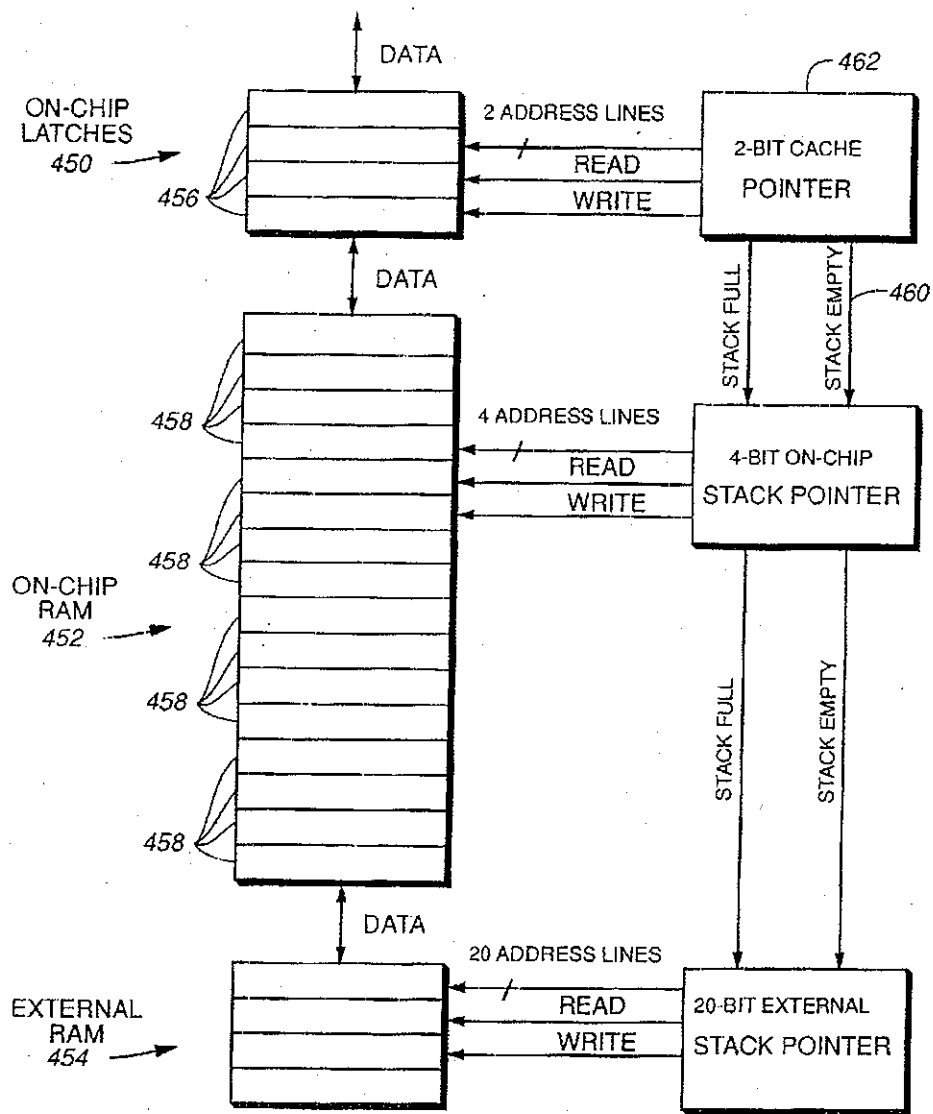


FIG. 21

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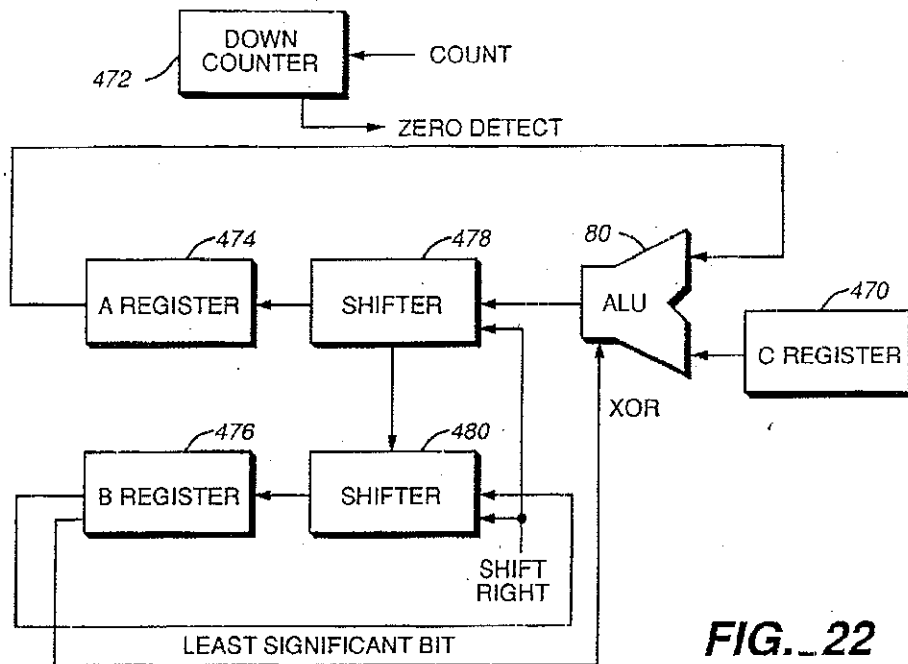


FIG. 22

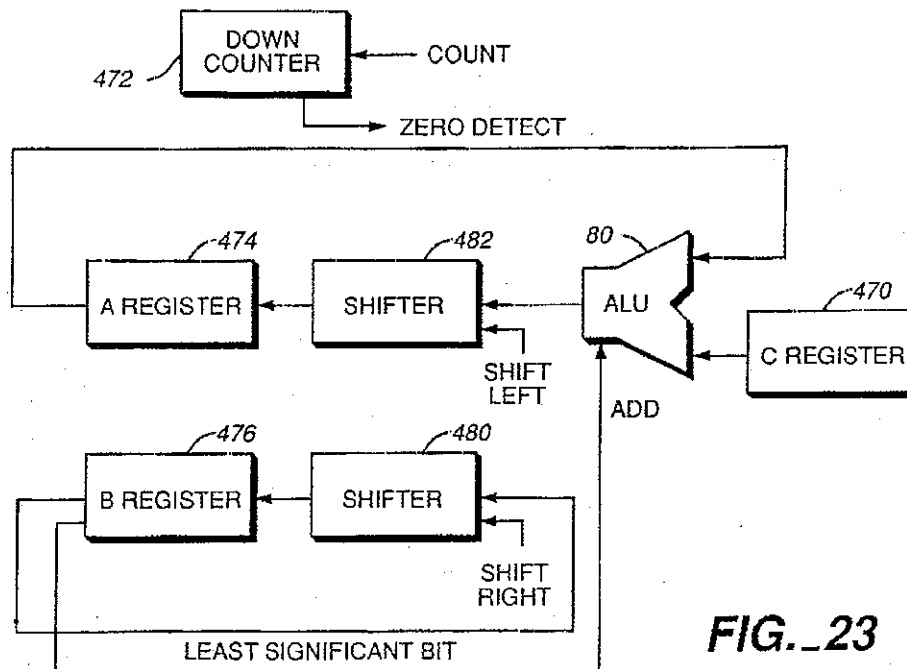


FIG. 23

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HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a division of U.S. application Ser No 07/389,334, filed Aug. 3, 1989, now U.S. Pat. No. 5,440,749

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to a simplified, reduced instruction set computer (RISC) microprocessor. More particularly, it relates to such a microprocessor which is capable of performance levels of, for example, 20 million instructions per second (MIPS) at a price of, for example, 20 dollars.

2. Description of the Prior Art

Since the invention of the microprocessor, improvements in its design have taken two different approaches. In the first approach, a brute force gain in performance has been achieved through the provision of greater numbers of faster transistors in the microprocessor integrated circuit and an instruction set of increased complexity. This approach is exemplified by the Motorola 68000 and Intel 80X86 microprocessor families. The trend in this approach is to larger die sizes and packages, with hundreds of pinouts.

More recently, it has been perceived that performance gains can be achieved through comparative simplicity, both in the microprocessor integrated circuit itself and in its instruction set. This second approach provides RISC microprocessors, and is exemplified by the Sun SPARC and the Intel 8960 microprocessors. However, even with this approach as conventionally practiced, the packages for the microprocessor are large, in order to accommodate the large number of pinouts that continue to be employed. A need therefore remains for further simplification of high performance microprocessors.

With conventional high performance microprocessors, fast static memories are required for direct connection to the microprocessors in order to allow memory accesses that are fast enough to keep up with the microprocessors. Slower dynamic random access memories (DRAMs) are used with such microprocessors only in a hierarchical memory arrangement, with the static memories acting as a buffer between the microprocessors and the DRAMs. The necessity to use static memories increases cost of the resulting systems.

Conventional microprocessors provide direct memory accesses (DMA) for system peripheral units through DMA controllers, which may be located on the microprocessor integrated circuit, or provided separately. Such DMA controllers can provide routine handling of DMA requests and responses, but some processing by the main central processing unit (CPU) of the microprocessor is required.

SUMMARY OF THE INVENTION

Accordingly, it is an object of this invention to provide a microprocessor with a reduced pin count and cost compared to conventional microprocessors.

It is another object of the invention to provide a high performance microprocessor that can be directly connected to DRAMs without sacrificing microprocessor speed.

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It is a further object of the invention to provide a high performance microprocessor in which DMA does not require use of the main CPU during DMA requests and responses and which provides very rapid DMA response with predictable response times.

The attainment of these and related objects may be achieved through use of the novel high performance, low cost microprocessor herein disclosed. In accordance with one aspect of the invention, a microprocessor system in accordance with this invention has a central processing unit, a dynamic random access memory and a bus connecting the central processing unit to the dynamic random access memory. There is a multiplexing means on the bus between the central processing unit and the dynamic random access memory. The multiplexing means is connected and configured to provide row addresses, column addresses and data on the bus.

In accordance with another aspect of the invention, the microprocessor system has a means connected to the bus for fetching instructions for the central processing unit on the bus. The means for fetching instructions is configured to fetch multiple sequential instructions in a single memory cycle. In a variation of this aspect of the invention, a programmable read only memory containing instructions for the central processing unit is connected to the bus. The means for fetching instructions includes means for assembling a plurality of instructions from the programmable read only memory and storing the plurality of instructions in the dynamic random access memory.

In another aspect of the invention, the microprocessor system includes a central processing unit, a direct memory access processing unit and a memory connected by a bus. The direct memory access processing unit includes means for fetching instructions for the central processing unit and for fetching instructions for the direct memory access processing unit on the bus.

In a further aspect of the invention, the microprocessor system, including the memory, is contained in an integrated circuit. The memory is a dynamic random access memory, and the means for fetching multiple instructions includes a column latch for receiving the multiple instructions.

In still another aspect of the invention, the microprocessor system additionally includes an instruction register for the multiple instructions connected to the means for fetching instructions. A means is connected to the instruction register for supplying the multiple instructions in succession from the instruction register. A counter is connected to control the means for supplying the multiple instructions to supply the multiple instructions in succession. A means for decoding the multiple instructions is connected to receive the multiple instructions in succession from the means for supplying the multiple instructions. The counter is connected to said means for decoding to receive incrementing and reset control signals from the means for decoding. The means for decoding is configured to supply the reset control signal to the counter and to supply a control signal to the means for fetching instructions in response to a SKIP instruction in the multiple instructions. In a modification of this aspect of the invention, the microprocessor system additionally has a loop counter connected to receive a decrement control signal from the means for decoding. The means for decoding is configured to supply the reset control signal to the counter and the decrement control signal to the loop counter in response to a MICROLOOP instruction in the multiple instructions. In a further modification to this aspect of the invention, the means for decoding is configured to control

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the counter in response to an instruction utilizing a variable width operand. A means is connected to the counter to select the variable width operand in response to the counter.

In a still further aspect of the invention, the microprocessor system includes an arithmetic logic unit. A first push down stack is connected to the arithmetic logic unit. The first push down stack includes means for storing a top item connected to a first input of the arithmetic logic unit and means for storing a next item connected to a second input of the arithmetic logic unit. The arithmetic logic unit has an output connected to the means for storing a top item. The means for storing a top item is connected to provide an input to a register file. The register file desirably is a second push down stack, and the means for storing a top item and the register file are bidirectionally connected.

In another aspect of the invention, a data processing system has a microprocessor including a sensing circuit and a driver circuit, a memory, and an output enable line connected between the memory, the sensing circuit and the driver circuit. The sensing circuit is configured to provide a ready signal when the output enable line reaches a predetermined electrical level, such as a voltage. The microprocessor is configured so that the driver circuit provides an enabling signal on the output enable line responsive to the ready signal.

In a further aspect of the invention, the microprocessor system has a ring counter variable speed system clock connected to the central processing unit. The central processing unit and the ring counter variable speed system clock are provided in a single integrated circuit. An input/output interface is connected to exchange coupling control signals, addresses and data with the input/output interface. A second clock independent of the ring counter variable speed system clock is connected to the input/output interface.

In yet another aspect of the invention, a push down stack is connected to the arithmetic logic unit. The push down stack includes means for storing a top item connected to a first input of the arithmetic logic unit and means for storing a next item connected to a second input of the arithmetic logic unit. The arithmetic logic unit has an output connected to the means for storing a top item. The push down stack has a first plurality of stack elements configured as latches and a second plurality of stack elements configured as a random access memory. The first and second plurality of stack elements and the central processing unit are provided in a single integrated circuit. A third plurality of stack elements is configured as a random access memory external to the single integrated circuit. In this aspect of the invention, desirably a first pointer is connected to the first plurality of stack elements, a second pointer connected to the second plurality of stack elements, and a third pointer is connected to the third plurality of stack elements. The central processing unit is connected to pop items from the first plurality of stack elements. The first stack pointer is connected to the second stack pointer to pop a first plurality of items from the second plurality of stack elements when the first plurality of stack elements are empty from successive pop operations by the central processing unit. The second stack pointer is connected to the third stack pointer to pop a second plurality of items from the third plurality of stack elements when the second plurality of stack elements are empty from successive pop operations by the central processing unit.

In another aspect of the invention, a first register is connected to supply a first input to the arithmetic logic unit. A first shifter is connected between an output of the arithmetic logic unit and the first register. A second register is

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connected to receive a starting polynomial value. An output of the second register is connected to a second shifter. A least significant bit of the second register is connected to The arithmetic logic unit. A third register is connected to supply feedback terms of a polynomial to the arithmetic logic unit. A down counter, for counting down a number corresponding to digits of a polynomial to be generated, is connected to the arithmetic logic unit. The arithmetic logic unit is responsive to a polynomial instruction to carry out an exclusive OR of the contents of the first register with the contents of the third register if the least significant bit of the second register is a "ONE" and to pass the contents of the first register unaltered if the least significant bit of the second register is a "ZERO", until the down counter completes a count. The polynomial to be generated results in said first register.

In still another aspect of the invention, a result register is connected to supply a first input to the arithmetic logic unit. A first, left shifting shifter is connected between an output of the arithmetic logic unit and the result register. A multiplier register is connected to receive a multiplier in bit reversed form. An output of the multiplier register is connected to a second, right shifting shifter. A least significant bit of the multiplier register is connected to the arithmetic logic unit. A third register is connected to supply a multiplicand to said arithmetic logic unit. A down counter, for counting down a number corresponding to one less than the number of digits of the multiplier, is connected to the arithmetic logic unit. The arithmetic logic unit is responsive to a multiply instruction to add the contents of the result register with the contents of the third register, when the least significant bit of the multiplier register is a "ONE" and to pass the contents of the result register unaltered, until the down counter completes a count. The product results in the result register.

The attainment of the foregoing and related objects, advantages and features of the invention should be more readily apparent to those skilled in the art, after review of the following more detailed description of the invention, taken together with the drawings, in which:

BRIEF DESCRIPTION OF THE DRAWINGS

FIG 1 is an external, plan view of an integrated circuit package incorporating a microprocessor in accordance with the invention.

FIG 2 is a block diagram of a microprocessor in accordance with the invention.

FIG 3 is a block diagram of a portion of a data processing system incorporating the microprocessor of FIGS. 1 and 2.

FIG 4 is a more detailed block diagram of a portion of the microprocessor shown in FIG. 2.

FIG 5 is a more detailed block diagram of another portion of the microprocessor shown in FIG. 2.

FIG. 6 is a block diagram of another portion of the data processing system shown in part in FIG. 3 and incorporating the microprocessor of FIGS. 1-2 and 4-5.

FIGS. 7 and 8 are layout diagrams for the data processing system shown in part in FIGS. 3 and 6.

FIG. 9 is a layout diagram of a second embodiment of a microprocessor in accordance with the invention in a data processing system on a single integrated circuit.

FIG 10 is a more detailed block diagram of a portion of the data processing system of FIGS. 7 and 8.

FIG. 11 is a timing diagram useful for understanding operation of the system portion shown in FIG. 12.

FIG 12 is another more detailed block diagram of a further portion of the data processing system of FIGS. 7 and 8.

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FIG 13 is a more detailed block diagram of a portion of the microprocessor shown in FIG 2

FIG 14 is a more detailed block and schematic diagram of a portion of the system shown in FIGS 3 and 7-8

FIG 15 is a graph useful for understanding operation of the system portion shown in FIG 14

FIG 16 is a more detailed block diagram showing part of the system portion shown in FIG 4

FIG 17 is a more detailed block diagram of a portion of the microprocessor shown in FIG 2

FIG 18 is a more detailed block diagram of part of the microprocessor portion shown in FIG 17

FIG 19 is a set of waveform diagrams useful for understanding operation of the part of the microprocessor portion shown in FIG 18

FIG 20 is a more detailed block diagram showing another part of the system portion shown in FIG 4

FIG 21 is a more detailed block diagram showing another part of the system portion shown in FIG 4

FIGS 22 and 23 are more detailed block diagrams showing another part of the system portion shown in FIG 4

DETAILED DESCRIPTION OF THE INVENTION

Overview

The microprocessor of this invention is desirably implemented as a 32-bit microprocessor optimized for:

HIGH EXECUTION SPEED and

LOW SYSTEM COST.

In this embodiment, the microprocessor can be thought of as 20 MIPS for 20 dollars. Important distinguishing features of the microprocessor are:

Uses low-cost commodity DYNAMIC RAMS to run 20 MIPS

4 instruction fetch per memory cycle

On-chip fast page-mode memory management

Runs fast without external cache

Requires few interfacing chips

Crams 32-bit CPU in 44 pin SOJ package

The instruction set is organized so that most operations can be specified with 8-bit instructions. Two positive products of this philosophy are:

Programs are smaller,

Programs can execute much faster

The bottleneck in most computer systems is the memory bus. The bus is used to fetch instructions and fetch and store data. The ability to fetch four instructions in a single memory bus cycle significantly increases the bus availability to handle data.

Turning now to the drawings, more particularly to FIG 1, there is shown a packaged 32-bit microprocessor 50 in a 44-pin plastic leadless chip carrier, shown approximately 100 times its actual size of about 0.8 inch on a side. The fact that the microprocessor 50 is provided as a 44-pin package represents a substantial departure from typical microprocessor packages, which usually have about 200 input/output (I/O) pins. The microprocessor 50 is rated at 20 million instructions per second (MIPS). Address and data lines 52, also labelled D0-D31, are shared for addresses and data without speed penalty as a result of the manner in which the microprocessor 50 operates, as will be explained below.

DYNAMIC RAM

In addition to the low cost 44-pin package, another unusual aspect of the high performance microprocessor 50 is

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that it operates directly with dynamic random access memories (DRAMs), as shown by row address strobe (RAS) and column address strobe (CAS) I/O pins 54. The other I/O pins for the microprocessor 50 include V_{DD} pins 56, V_{SS} pins 58, output enable pin 60, write pin 62, clock pin 64 and reset pin 66.

All high speed computers require high speed and expensive memory to keep up. The highest speed static RAM memories cost as much as ten times as much as slower dynamic RAMs. This microprocessor has been optimized to use low-cost dynamic RAM in high-speed page-mode. Page-mode dynamic RAMs offer static RAM performance without the cost penalty. For example, low-cost 85 nsec. dynamic RAMs access at 25 nsec when operated in fast page-mode. Integrated fast page-mode control on the microprocessor chip simplifies system interfacing and results in a faster system.

Details of the microprocessor 50 are shown in FIG 2. The microprocessor 50 includes a main central processing unit (CPU) 70 and a separate direct memory access (DMA) CPU 72 in a single integrated circuit making up the microprocessor 50. The main CPU 70 has a first 16 deep push down stack 74, which has a top item register 76 and a next item register 78, respectively connected to provide inputs to an arithmetic logic unit (ALU) 80 by lines 82 and 84. An output of the ALU 80 is connected to the top item register 76 by line 86. The output of the top item register at 82 is also connected by line 88 to an internal data bus 90.

A loop counter 92 is connected to a decrements 94 by lines 96 and 98. The loop counter 92 is bidirectionally connected to the internal data bus 90 by line 100. Stack pointer 102, return stack pointer 104, mode register 106 and instruction register 108 are also connected to the internal data bus 90 by lines 110, 112, 114 and 116, respectively. The internal data bus 90 is connected to memory controller 118 and to gate 120. The gate 120 provides inputs on lines 122, 124, and 126 to X register 128, program counter 130 and Y register 132 of return push down stack 134. The X register 128, program counter 130 and Y register 132 provide outputs to internal address bus 136 on lines 138, 140 and 142. The internal address bus provides inputs to the memory controller 118 and to an incrementer 144. The incrementer 144 provides inputs to the X register, program counter and Y register via lines 146, 122, 124 and 126. The DMA CPU 72 provides inputs to the memory controller 118 on line 148. The memory controller 118 is connected to a RAM (not shown) by address/data bus 150 and control lines 152.

FIG 2 shows that the microprocessor 50 has a simple architecture. Prior art RISC microprocessors are substantially more complex in design. For example, the SPARC RISC microprocessor has three times the gates of the microprocessor 50, and the Intel 8960 RISC microprocessor has 20 times the gates of the microprocessor 50. The speed of this microprocessor is in substantial part due to this simplicity. The architecture incorporates push down stacks and register write to achieve this simplicity.

The microprocessor 50 incorporates an I/O that has been tuned to make heavy use of resources provided on the integrated circuit chip. On chip latches allow use of the same I/O circuits to handle three different things: column addressing, row addressing and data, with a slight to non-existent speed penalty. This triple bus multiplexing results in fewer buffers to expand, fewer interconnection lines, fewer I/O pins and fewer internal buffers.

The provision of on-chip DRAM control gives a performance equal to that obtained with the use of static RAMs. As a result, memory is provided at 1/4 the system cost of static RAM used in most RISC systems.

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The microprocessor 50 fetches 4 instructions per memory cycle; the instructions are in an 8-bit format, and this is a 32-bit microprocessor. System speed is therefore 4 times the memory bus bandwidth. This ability enables the microprocessor to break the Von Neumann bottleneck of the speed of getting the next instruction. This mode of operation is possible because of the use of a push down stack and register array. The push down stack allows the use of implied addresses, rather than the prior art technique of explicit addresses for two sources and a destination.

Most instructions execute in 20 nanoseconds in the microprocessor 50. The microprocessor can therefore execute instructions at 50 peak MIPS without pipeline delays. This is a function of the small number of gates in the microprocessor 50 and the high degree of parallelism in the architecture of the microprocessor.

FIG 3 shows how column and row addresses are multiplexed on lines D8-D14 of the microprocessor 50 for addressing DRAM 150 from I/O pins 52. The DRAM 150 is one of eight, but only one DRAM 150 has been shown for clarity. As shown, the lines D11-D18 are respectively connected to row address inputs A0-A8 of the DRAM 150. Additionally, lines D12-D15 are connected to the data inputs DQ1-DQ4 of the DRAM 150. The output enable, write and column address strobe pins 54 are respectively connected to the output enable, write and column address strobe inputs of the DRAM 150 by lines 152. The row address strobe pin 54 is connected through row address strobe decode logic 154 to the row address strobe input of the DRAM 150 by lines 156 and 158.

D0-D7 pins 52 (FIG 1) are idle when the microprocessor 50 is outputting multiplexed row and column addresses on D11-D18 pins 52. The D0-D7 pins 52 can therefore simultaneously be used for I/O when not justified I/O is desired. Simultaneous addressing and I/O can therefore be carried out.

FIG 4 shows how the microprocessor 50 is able to achieve performance equal to the use of static RAMS with DRAMs through multiple instruction fetch in a single clock cycle and instruction fetch-ahead. Instruction register 108 receives four 8-bit byte instruction words 1-4 on 32-bit internal data bus 90. The four instruction byte 1-4 locations of the instruction register 108 are connected to multiplexer 170 by busses 172, 174, 176 and 178, respectively. A microprogram counter 180 is connected to the multiplexer 170 by lines 182. The multiplexer 170 is connected to decoder 184 by bus 186. The decoder 184 provides internal signals to the rest of the microprocessor 50 on lines 188.

Most significant bits 190 of each instruction byte 1-4 location are connected to a 4-input decoder 192 by lines 194. The output of decoder 192 is connected to memory controller 118 by line 196. Program counter 130 is connected to memory controller 118 by internal address bus 136, and the instruction register 108 is connected to the memory controller 118 by the internal data bus 90. Address/data bus 198 and control bus 200 are connected to the DRAMs 150 (FIG 3).

In operation, when the most significant bits 190 of remaining instructions 1-4 are "1" in a clock cycle of the microprocessor 50, there are no memory reference instructions in the queue. The output of decoder 192 on line 196 requests an instruction fetch ahead by memory controller 118 without interference with other accesses. While the current instructions in instruction register 108 are executing, the memory controller 118 obtains the address of the next set of four instructions from program counter 130 and obtains that set of instructions. By the time the current set of instructions has completed execution, the next set of instructions is ready for loading into the instruction register.

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Details of the DMA CPU 72 are provided in FIG. 5. Internal data bus 90 is connected to memory controller 118 and to DMA instruction register 210. The DMA instruction register 210 is connected to DMA program counter 212 by bus 214, to transfer size counter 216 by bus 218 and to timed transfer interval counter 220 by bus 222. The DMA instruction register 210 is also connected to DMA I/O and RAM address register 224 by line 226. The DMA I/O and RAM address register 224 is connected to the memory controller 118 by memory cycle request line 228 and bus 230. The DMA program counter 212 is connected to the internal address bus 136 by bus 232. The transfer size counter 216 is connected to a DMA instruction done decremter 234 by lines 236 and 238. The decremter 234 receives a control input on memory cycle acknowledge line 240. When transfer size counter 216 has completed its count, it provides a control signal to DMA program counter 212 on line 242. Timed transfer interval counter 220 is connected to decremter 244 by lines 246 and 248. The decremter 244 receives a control input from a microprocessor system clock on line 250.

The DMA CPU 72 controls itself and has the ability to fetch and execute instructions. It operates as a co-processor to the main CPU 70 (FIG 2) for time specific processing.

FIG 6 shows how the microprocessor 50 is connected to an electrically programmable read only memory (EPROM) 260 by reconfiguring the data lines 52 so that some of the data lines 52 are input lines and some of them are output lines. Data lines 52 D0-D7 provide data to and from corresponding data terminals 262 of the EPROM 260. Data lines 52 D9-D18 provide addresses to address terminals 264 of the EPROM 260. Data lines 52 D19-D31 provide inputs from the microprocessor 50 to memory and I/O decode logic 266. RAS 0/1 control line 268 provides a control signal for determining whether the memory and I/O decode logic provides a DRAM RAS output on line 270 or a column enable output for the EPROM 260 on line 272. Column address strobe terminal 60 of the microprocessor 50 provides an output enable signal on line 274 to the corresponding terminal 276 of the EPROM 260.

FIGS 7 and 8 show the front and back of a one card data processing system 280 incorporating the microprocessor 50, MSM514258-10 type DRAMs 150 totalling 2 megabytes, a Motorola 50 MegaHertz crystal oscillator clock 282, I/O circuits 284 and a 27256 type EPROM 260. The I/O circuits 284 include a 74HC04 type high speed hex inverter circuit 286, an IDT39C828 type 10-bit inverting buffer circuit 288, an IDT39C822 type 10-bit inverting register circuit 290, and two IDT39C823 type 9-bit non-inverting register circuits 292. The card 280 is completed with a MAX12V type DC-DC converter circuit 294, 34-pin dual AMP type headers 296, a coaxial female power connector 298, and a 3-pin AMP right angle header 300. The card 280 is a low cost, imbeddable product that can be incorporated in larger systems or used as an internal development tool.

The microprocessor 50 is a very high performance (50 MHz) RISC influenced 32-bit CPU designed to work closely with dynamic RAM. Clock for clock, the microprocessor 50 approaches the theoretical performance limits possible with a single CPU configuration. Eventually, the microprocessor 50 and any other processor is limited by the bus bandwidth and the number of bus paths. The critical conduit is between the CPU and memory.

One solution to the bus bandwidth/bus path problem is to integrate a CPU directly onto the memory chips, giving every memory a direct bus to the CPU. FIG 9 shows another microprocessor 310 that is provided integrally with 1 mega-

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bit of DRAM 311 in a single integrated circuit 312. Until the present invention, this solution has not been practical, because most high performance CPUs require from 500,000 to 1,000,000 transistors and enormous die sizes just by themselves. The microprocessor 310 is equivalent to the microprocessor 50 in FIGS 1-8. The microprocessors 50 and 310 are the most transistor efficient high performance CPUs in existence, requiring fewer than 50,000 transistors for dual processors 70 and 72 (FIG 2) or 314 and 316 (less memory). The very high speed of the microprocessors 50 and 310 is to a certain extent a function of the small number of active devices. In essence, the less silicon gets in the way, the faster the electrons can get where they are going.

The microprocessor 310 is therefore the only CPU suitable for integration on the memory chip die 312. Some simple modifications to the basic microprocessor 50 to take advantage of the proximity to the DRAM array 311 can also increase the microprocessor 50 clock speed by 50 percent, and probably more.

The microprocessor 310 core on board the DRAM die 312 provides most of the speed and functionality required for a large group of applications from automotive to peripheral control. However, the integrated CPU 310/DRAM 311 concept has the potential to redefine significantly the way multiprocessor solutions can solve a spectrum of very compute intensive problems. The CPU 310/DRAM 311 combination eliminates the Von Neumann bottleneck by distributing it across numerous CPU/DRAM chips 312. The microprocessor 310 is a particularly good core for multiprocessing, since it was designed with the SDI targeting array in mind, and provisions were made for efficient interprocessor communications.

Traditional multiprocessor implementations have been very expensive in addition to being unable to exploit fully the available CPU horsepower. Multiprocessor systems have typically been built up from numerous board level or box level computers. The result is usually an immense amount of hardware with corresponding wiring, power consumption and communications problems. By the time the systems are interconnected, as much as 50 percent of the bus speed has been utilized just getting through the interfaces.

In addition, multiprocessor system software has been scarce. A multiprocessor system can easily be crippled by an inadequate load-sharing algorithm in the system software, which allows one CPU to do a great deal of work and the others to be idle. Great strides have been made recently in systems software, and even UNIX V4 may be enhanced to support multiprocessing. Several commercial products from such manufacturers as DUAL Systems and UNISOFT do a credible job on 68030 type microprocessor systems now.

The microprocessor 310 architecture eliminates most of the interface friction, since up to 64 CPU 310/RAM 311 processors should be able to intercommunicate without buffers or latches. Each chip 312 has about 40 MIPS raw speed, because placing the DRAM 311 next to the CPU 310 allows the microprocessor 310 instruction cycle to be cut in half, compared to the microprocessor 50. A 64 chip array of these chips 312 is more powerful than any other existing computer. Such an array fits on a 3x5 card, cost less than a FAX machine, and draw about the same power as a small television.

Dramatic changes in price/performance always reshape existing applications and almost always create new ones. The introduction of microprocessors in the mid 1970s created video games, personal computers, automotive computers, electronically controlled appliances, and low cost computer peripherals.

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The integrated circuit 312 will find applications in all of the above areas, plus create some new ones. A common generic parallel processing algorithm handles convolution/Fast Fourier Transform (FFT)/pattern recognition. Interesting product possibilities using the integrated circuit 312 include high speed reading machines, real-time speech recognition, spoken language translation, real-time robot vision, a product to identify people by their faces, and an automotive or aviation collision avoidance system.

A real time processor for enhancing high density television (HDTV) images, or compressing the HDTV information into a smaller bandwidth, would be very feasible. The load sharing in HDTV could be very straightforward. Splitting up the task according to color and frame would require 6, 9 or 12 processors. Practical implementation might require 4 meg RAMs integrated with the microprocessor 310.

The microprocessor 310 has the following specifications:

CONTROL LINES

4—POWER/GROUND

1—CLOCK

32—DATA I/O

4—SYSTEM CONTROL

EXTERNAL MEMORY FETCH

EXTERNAL MEMORY FETCH AUTOINCREMENT X

EXTERNAL MEMORY FETCH AUTOINCREMENT Y

EXTERNAL MEMORY WRITE

EXTERNAL MEMORY WRITE AUTOINCREMENT X

EXTERNAL MEMORY WRITE AUTOINCREMENT Y

EXTERNAL PROM FETCH

LOAD ALL X REGISTERS

LOAD ALL Y REGISTERS

LOAD ALL PC REGISTERS

EXCHANGE X AND Y

INSTRUCTION FETCH

ADD TO PC

ADD TO X

WRITE MAPPING REGISTER

READ MAPPING REGISTER

REGISTER CONFIGURATION

MICROPROCESSOR 310 CPU 316 CORE

COLUMN LATCH1 (1024 BITS) 32x32 MUX

STACK POINTER (16 BITS)

COLUMN LATCH2 (1024 BITS) 32x32 MUX

RSTACK POINTER (16 BITS)

PROGRAM COUNTER 32 BITS

X0 REGISTER 32 BITS (ACTIVATED ONLY FOR ON-CHIP ACCESSES)

Y0 REGISTER 32 BITS (ACTIVATED ONLY FOR ON-CHIP ACCESSES)

LOOP COUNTER 32 BITS

DMA CPU 314 CORE

DMA PROGRAM COUNTER 24 BITS

INSTRUCTION REGISTER 32 BITS

I/O & RAM ADDRESS REGISTER 32 BITS

TRANSFER SIZE COUNTER 12 BITS

INTERVAL COUNTER 12 BITS

To offer memory expansion for the basic chip 312, an intelligent DRAM can be produced. This chip will be optimized for high speed operation with the integrated circuit 312 by having three on-chip address registers: Program Counter, X Register and Y register. As a result, to access the intelligent DRAM, no address is required, and a total access cycle could be as short as 10 nsec. Each

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expansion DRAM would maintain its own copy of the three registers and would be identified by a code specifying its memory address. Incrementing and adding to the three registers will actually take place on the memory chips. A maximum of 64 intelligent DRAM peripherals would allow a large system to be created without sacrificing speed by introducing multiplexers or buffers.

There are certain differences between the microprocessor 310 and the microprocessor 50 that arise from providing the microprocessor 310 on the same die 312 with the DRAM 311. Integrating the DRAM 311 allows architectural changes in the microprocessor 310 logic to take advantage of existing on-chip DRAM 311 circuitry. Row and column design is inherent in memory architecture. The DRAMs 311 access random bits in a memory array by first selecting a row of 1024 bits, storing them into a column latch, and then selecting one of the bits as the data to be read or written.

The time required to access the data is split between the row access and the column access. Selecting data already stored in a column latch is faster than selecting a random bit by at least a factor of six. The microprocessor 310 takes advantage of this high speed by creating a number of column latches and using them as caches and shift registers. Selecting a new row of information may be thought of as performing a 1024-bit read or write with the resulting immense bus bandwidth.

1. The microprocessor 50 treats its 32-bit instruction register 108 (see FIGS. 2 and 4) as a cache for four 8-bit instructions. Since the DRAM 311 maintains a 1024-bit latch for the column bits, the microprocessor 310 treats the column latch as a cache for 128 8-bit instructions. Therefore, the next instruction will almost always be already present in the cache. Long loops within the cache are also possible and more useful than the 4 instruction loops in the microprocessor 50.

2. The microprocessor 50 uses two 16x32-bit deep register arrays 74 and 134 (FIG. 2) for the parameter stack and the return stack. The microprocessor 310 creates two other 1024-bit column latches to provide the equivalent of two 32x32-bit arrays, which can be accessed twice as fast as a register array.

3. The microprocessor 50 has a DMA capability which can be used for I/O to a video shift register. The microprocessor 310 uses yet another 1024-bit column latch as a long video shift register to drive a CRI display directly. For color displays, three on-chip shift registers could also be used. These shift registers can transfer pixels at a maximum of 100 MHz.

4. The microprocessor 50 accesses memory via an external 32-bit bus. Most of the memory 311 for the microprocessor 310 is on the same die 312. External access to more memory is made using an 8-bit bus. The result is a smaller die, smaller package and lower power consumption than the microprocessor 50.

5. The microprocessor 50 consumes about a third of its operating power charging and discharging the I/O pins and associated capacitances. The DRAMs 150 (FIG. 8) connected to the microprocessor 50 dissipate most of their power in the I/O drivers. A microprocessor 310 system will consume about one-tenth the power of a microprocessor 50 system, since having the DRAM 311 next to the processor 310 eliminates most of the external capacitances to be charged and discharged.

6. Multiprocessing means splitting a computing task between numerous processors in order to speed up the solution. The popularity of multiprocessing is limited by the expense of current individual processors as well as the

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limited interprocessor communications ability. The microprocessor 310 is an excellent multiprocessor candidate, since the chip 312 is a monolithic computer complete with memory, rendering it low-cost and physically compact.

The shift registers implemented with the microprocessor 310 to perform video output can also be configured as interprocessor communication links. The INMOS transputer attempted a similar strategy, but at much lower speed and without the performance benefits inherent in the microprocessor 310 column latch architecture. Serial I/O is a prerequisite for many multiprocessor topologies because of the many neighbor processors which communicate. A cube has 6 neighbors. Each neighbor communicates using these lines:

DATA IN
CLOCK IN
READY FOR DATA
DATA OUT
DATA READY?
CLOCK OUT

A special start up sequence is used to initialize the on-chip DRAM 311 in each of the processors.

The microprocessor 310 column latch architecture allows neighbor processors to deliver information directly to internal registers or even instruction caches of other chips 312. This technique is not used with existing processors, because it only improves performance in a tightly coupled DRAM system.

7. The microprocessor 50 architecture offers two types of looping structures: LOOP-IF-DONE and MICRO-LOOP. The former takes an 8-bit to 24-bit operand to describe the entry point to the loop address. The latter performs a loop entirely within the 4 instruction queue and the loop entry point is implied as the first instruction in the queue. Loops entirely within the queue run without external instruction fetches and execute up to three times as fast as the long loop construct. The microprocessor 310 retains both constructs with a few differences. The microprocessor 310 microloop functions in the same fashion as the microprocessor 50 operation, except the queue is 1024-bits or 128 8-bit instructions long. The microprocessor 310 microloop can therefore contain jumps, branches, calls and immediate operations not possible in the 4 8-bit instruction microprocessor 50 queue.

Microloops in the microprocessor 50 can only perform simple block move and compare functions. The larger microprocessor 310 queue allows entire digital signal processing or floating point algorithms to loop at high speed in the queue.

The microprocessor 50 offers four instructions to redirect execution:

CALL
BRANCH
BRANCH-IF-ZERO
LOOP-IF-NOT-DONE

These instructions take a variable length address operand 8, 16 or 24 bits long. The microprocessor 50 next address logic treats the three operands similarly by adding or subtracting them to the current program counter. For the microprocessor 310, the 16 and 24-bit operands function in the same manner as the 16 and 24-bit operands in the microprocessor 50. The 8-bit class operands are reserved to operate entirely within the instruction queue. Next address decisions can therefore be made quickly, because only 10 bits of addresses are affected, rather than 32. There is no carry or borrow generated past the 10 bits.

8. The microprocessor 310 CPU 316 resides on an already crowded DRAM die 312. To keep chip size as small as

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possible, the DMA processor 72 of the microprocessor 50 has been replaced with a more traditional DMA controller 314. DMA is used with the microprocessor 310 to perform the following functions:

Video output to a CRI

Multiprocessor serial communications

8-bit parallel I/O

The DMA controller 314 can maintain both serial and parallel transfers simultaneously. The following DMA sources and destinations are supported by the microprocessor 310:

DESCRIPTION	I/O	LINES
1 Video shift register	OUTPUT	1 to 3
2 Multiprocessor serial	BOTH	6 lines/channel
3 8-bit parallel	BOTH	8 data, 4 control

The three sources use separate 1024-bit buffers and separate I/O pins. Therefore, all three may be active simultaneously without interference.

The microprocessor 310 can be implemented with either a single multiprocessor serial buffer or separate receive and sending buffers for each channel, allowing simultaneous bidirectional communications with six neighbors simultaneously.

FIGS 10 and 11 provide details of the PROM DMA used in the microprocessor 50. The microprocessor 50 executes faster than all but the fastest PROMs. PROMs are used in a microprocessor 50 system to store program segments and perhaps entire programs. The microprocessor 50 provides a feature on power-up to allow programs to be loaded from low-cost, slow speed PROMs into high speed DRAM for execution. The logic which performs this function is part of the DMA memory controller 118. The operation is similar to DMA, but not identical, since four 8-bit bytes must be assembled on the microprocessor 50 chip, then written to the DRAM 150.

The microprocessor 50 directly interfaces to DRAM 150 over a triple multiplexed data and address bus 350, which carries RAS addresses, CAS addresses and data. The EPROM 260, on the other hand, is read with non-multiplexed busses. The microprocessor 50 therefore has a special mode which unmultiplexes the data and address lines to read 8 bits of EPROM data. Four 8-bit bytes are read in this fashion. The multiplexed bus 350 is turned back on, and the data is written to the DRAM 150.

When the microprocessor 50 detects a RESET condition, the processor stops the main CPU 70 and forces a mode 0 (PROM LOAD) instruction into the DMA CPU 72 instruction register. The DMA instruction directs the memory controller to read the EPROM 260 data at 8 times the normal access time for memory. Assuming a 50 MHz microprocessor 50, this means an access time of 320 nsec. The instruction also indicates:

The selection address of the EPROM 260 to be loaded,

The number of 32-bit words to transfer,

The DRAM 150 address to transfer into

The sequence of activities to transfer one 32-bit word from EPROM 260 to DRAM 150 are:

1 RAS goes low at 352, latching the EPROM 260 select information from the high order address bits. The EPROM 260 is selected.

2 Twelve address bits (consisting of what is normally DRAM CAS addresses plus two byte select bits are placed on the bus 350 going to the EPROM 260 address

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pins. These signals will remain on the lines until the data from the EPROM 260 has been read into the microprocessor 50. For the first byte, the byte select bits will be binary 00.

3 CAS goes low at 354, enabling the EPROM 260 data onto the lower 8 bits of the external address/data bus 350. NOTE: It is important to recognize that, during this part of the cycle, the lower 8 bits of the external data/address bus are functioning as inputs, but the rest of the bus is still acting as outputs.

4 The microprocessor 50 latches these eight least significant bits internally and shifts them 8 bits left to shift them to the next significant byte position.

5 Steps 2, 3 and 4 are repeated with byte address 01.

6 Steps 2, 3 and 4 are repeated with byte address 10.

7 Steps 2, 3 and 4 are repeated with byte address 11.

8 CAS goes high at 356, taking the EPROM 260 off the data bus.

9 RAS goes high at 358, indicating the end of the EPROM 260 access.

10 RAS goes low at 360, latching the DRAM select information from the high order address bits. At the same time, the RAS address bits are latched into the DRAM 150. The DRAM 150 is selected.

11 CAS goes low at 362, latching the DRAM 150 CAS addresses.

12 The microprocessor 50 places the previously latched EPROM 260 32-bit data onto the external address/data bus 350. W goes low at 364, writing the 32 bits into the DRAM 150.

13 W goes high at 366. CAS goes high at 368. The process continues with the next word.

FIG. 12 shows details of the microprocessor 50 memory controller 118. In operation, bus requests stay present until they are serviced. CPU 70 requests are prioritized at 370 in the order of: 1, Parameter Stack; 2, Return Stack; 3, Data Fetch; 4, Instruction Fetch. The resulting CPU request signal and a DMA request signal are supplied as bus requests to bus control 372, which provides a bus grant signal at 374. Internal address bus 136 and a DMA counter 376 provide inputs to a multiplexer 378. Either a row address or a column address are provided as an output to multiplexed address bus 380 as an output from the multiplexer 378. The multiplexed address bus 380 and the internal data bus 90 provide address and data inputs, respectively, to multiplexer 382. Shift register 384 supplies row address strobe (RAS) 1 and 2 control signals to multiplexer 386 and column address strobe (CAS) 1 and 2 control signals to multiplexer 388 on lines 390 and 392. The shift register 384 also supplies output enable (OE) and write (W) signals on lines 394 and 396 and a control signal on line 398 to multiplexer 382. The shift register 384 receives a RUN signal on line 400 to generate a memory cycle and supplies a MEMORY READY signal on line 402 when an access is complete.

STACK/REGISTER ARCHITECTURE

Most microprocessors use on-chip registers for temporary storage of variables. The on-chip registers access data faster than off-chip RAM. A few microprocessors use an on-chip push down stack for temporary storage.

A stack has the advantage of faster operation compared to on-chip registers by avoiding the necessity to select source and destination registers. (A math or logic operation always uses the top two stack items as source and the top of stack as destination.) The stack's disadvantage is that it makes some operations clumsy. Some compiler activities in particular require on-chip registers for efficiency.

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As shown in FIG. 13, the microprocessor 50 provides both on-chip registers 134 and a stack 74 and reaps the benefits of both

BENEFITS:

- 1 Stack math and logic is twice as fast as those available on an equivalent register only machine. Most programmers and optimizing compilers can take advantage of this feature
- 2 Sixteen registers are available for on-chip storage of local variables which can transfer to the stack for computation. The accessing of variables is three to four times as fast as available on a strictly stack machine.

The combined stack 74/register 134 architecture has not been used previously due to inadequate understanding by computer designers of optimizing compilers and the mix of transfer versus math/logic instructions

ADAPTIVE MEMORY CONTROLLER

A microprocessor must be designed to work with small or large memory configurations. As more memory loads are added to the data, address, and control lines, the switching speed of the signals slows down. The microprocessor 50 multiplexes the address/data bus three ways, so timing between the phases is critical. A traditional approach to the problem allocates a wide margin of time between bus phases so that systems will work with small or large numbers of memory chips connected. A speed compromise of as much as 50% is required.

As shown in FIG. 14, the microprocessor 50 uses a feedback technique to allow the processor to adjust memory bus timing to be fast with small loads and slower with large ones. The OUTPUT ENABLE (OE) line 152 from the microprocessor 50 is connected to all memories 150 on the circuit board. The loading on the output enable line 152 to the microprocessor 50 is directly related to the number of memories 150 connected. By monitoring how rapidly OE 152 goes high after a read, the microprocessor 50 is able to determine when the data hold time has been satisfied and place the next address on the bus.

The level of the OE line 152 is monitored by CMOS input buffer 410 which generates an internal READY signal on line 412 to the microprocessor's memory controller. Curves 414 and 416 of the FIG. 15 graph show the difference in rise time likely to be encountered from a lightly to heavily loaded memory system. When the OE line 152 has reached a predetermined level to generate the READY signal, driver 418 generates an OUTPUT ENABLE signal on OE line 152.

SKIP WITHIN THE INSTRUCTION CACHE

The microprocessor 50 fetches four 8-bit instructions each memory cycle and stores them in a 32-bit instruction register 108, as shown in FIG. 16. A class of "test and skip" instructions can very rapidly execute a very fast jump operation within the four instruction cache

SKIP CONDITIONS:

Always
ACC non-zero
ACC negative
Carry flag equal logic one
Never
ACC equal zero
ACC positive
Carry flag equal logic zero

The SKIP instruction can be located in any of the four byte positions 420 in the 32-bit instruction register 108. If the test is successful, SKIP will jump over the remaining one, two, or three 8-bit instructions in the instruction register

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108 and cause the next four-instruction group to be loaded into the register 108. As shown, the SKIP operation is implemented by resetting the 2-bit microinstruction counter 180 to zero on line 422 and simultaneously latching the next instruction group into the register 108. Any instructions following the SKIP in the instruction register are overwritten by the new instructions and not executed.

The advantage of SKIP is that optimizing compilers and smart programmers can often use it in place of the longer conditional JUMP instruction. SKIP also makes possible microloops which exit when the loop counts down or when the SKIP jumps to the next instruction group. The result is very fast code.

Other machines (such as the PDP-8 and Data General NOVA) provide the ability to skip a single instruction. The microprocessor 50 provides the ability to skip up to three instructions.

MICROLOOP IN THE INSTRUCTION CACHE

The microprocessor 50 provides the MICROLOOP instruction to execute repetitively from one to three instructions residing in the instruction register 108. The microloop instruction works in conjunction with the LOOP COUNTER 92 (FIG. 2) connected to the internal data bus 90. To execute a microloop, the program stores a count in LOOP COUNTER 92. MICROLOOP may be placed in the first, second, third, or last byte 420 of the instruction register 108. If placed in the first position, execution will just create a delay equal to the number stored in LOOP COUNTER 92 times the machine cycle. If placed in the second, third, or last byte 420, when the microloop instruction is executed, it will test the LOOP COUNT for zero. If zero, execution will continue with the next instruction. If not zero, the LOOP COUNTER 92 is decremented and the 2-bit microinstruction counter is cleared, causing the preceding instructions in the instruction register to be executed again.

Microloop is useful for block move and search operations. By executing a block move completely out of the instruction register 108, the speed of the move is doubled, since all memory cycles are used by the move rather than being shared with instruction fetching. Such a hardware implementation of microloops is much faster than conventional software implementation of a comparable function.

OPTIMAL CPU CLOCK SCHEME

The designer of a high speed microprocessor must produce a product which operate over wide temperature ranges, wide voltage swings, and wide variations in semiconductor processing. Temperature, voltage, and process all affect transistor propagation delays. Traditional CPU designs are done so that with the worse case of the three parameters, the circuit will function at the rated clock speed. The result are designs that must be clocked a factor of two slower than their maximum theoretical performance, so they will operate properly in worse case conditions.

The microprocessor 50 uses the technique shown in FIGS. 17-19 to generate the system clock and its required phases. Clock circuit 430 is the familiar "ring oscillator" used to test process performance. The clock is fabricated on the same silicon chip as the rest of the microprocessor 50.

The ring oscillator frequency is determined by the parameters of temperature, voltage, and process. At room temperature, the frequency will be in the neighborhood of 100 MHz. At 70 degrees Centigrade, the speed will be 50 MHz. The ring oscillator 430 is useful as a system clock, with its stages 431 producing phase 0-phase 3 outputs 433 shown in FIG. 19, because its performance tracks the parameters which similarly affect all other transistors on the same silicon die. By deriving system timing from the ring

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oscillator 430, CPU 70 will always execute at the maximum frequency possible, but never too fast. For example, if the processing of a particular die is not good resulting in slow transistors, the latches and gates on the microprocessor 50 will operate slower than normal. Since the microprocessor 50 ring oscillator clock 430 is made from the same transistors on the same die as the latches and gates, it too will operate slower (oscillating at a lower frequency), providing compensation which allows the rest of the chip's logic to operate properly.

ASYNCHRONOUS/SYNCHRONOUS CPU

Most microprocessors derive all system timing from a single clock. The disadvantage is that different parts of the system can slow all operations. The microprocessor 50 provides a dual-clock scheme as shown in FIG. 17, with the CPU 70 operating a synchronously to I/O interface 432 forming part of memory controller 118 (FIG. 2) and the I/O interface 432 operating synchronously with the external world of memory and I/O devices. The CPU 70 executes at the fastest speed possible using the adaptive ring counter clock 430. Speed may vary by a factor of four depending upon temperature, voltage, and process. The external world must be synchronized to the microprocessor 50 for operations such as video display updating and disc drive reading and writing. This synchronization is performed by the I/O interface 432, speed of which is controlled by a conventional crystal clock 434. The interface 432 processes requests for memory accesses from the microprocessor 50 and acknowledges the presence of I/O data. The microprocessor 50 fetches up to four instructions in a single memory cycle and can perform much useful work before requiring another memory access. By decoupling the variable speed of the CPU 70 from the fixed speed of the I/O interface 432 optimum performance can be achieved by each. Recoupling between the CPU 70 and the interface 432 is accomplished with handshake signals on lines 436, with data/addresses passing on bus 90, 136.

ASYNCHRONOUS/SYNCHRONOUS CPU IMBEDDED ON A DRAM CHIP

System performance is enhanced even more when the DRAM 311 and CPU 314 (FIG. 9) are located on the same die. The proximity of the transistors means that DRAM 311 and CPU 314 parameters will closely follow each other. At room temperature, not only would the CPU 314 execute at 100 MHz, but the DRAM 311 would access fast enough to keep up. The synchronization performed by the I/O interface 432 would be for DMA and reading and writing I/O ports. In some systems (such as calculators) no I/O synchronization at all would be required, and the I/O clock would be tied to the ring counter clock.

VARIABLE WIDTH OPERANDS

Many microprocessors provide variable width operands. The microprocessor 50 handles operands of 8, 16, or 24 bits using the same op-code. FIG. 20 shows the 32-bit instruction register 108 and the 2-bit microinstruction register 180 which selects the 8-bit instruction. Two classes of microprocessor 50 instructions can be greater than 8-bits, JUMP class and IMMEDIATE A JUMP or IMMEDIATE op-code is 8-bits, but the operand can be 8, 16, or 24 bits long. This magic is possible because operands must be right justified in the instruction register. This means that the least significant bit of the operand is always located in the least significant bit of the instruction register. The microinstruction counter 180 selects which 8-bit instruction to execute. If a JUMP or IMMEDIATE instruction is decoded, the state of the 2-bit microinstruction counter selects the required 8, 16, or 24 bit operand onto the address or data bus. The unselected 8-bit

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bytes are loaded with zeros by operation of decoder 440 and gates 442. The advantage of this technique is the saving of a number of op-codes required to specify the different operand sizes in other microprocessors.

TRIPLE STACK CACHE

Computer performance is directly related to the system memory bandwidth. The faster the memories the faster the computer. Fast memories are expensive, so techniques have been developed to move a small amount of high-speed memory around to the memory addresses where it is needed. A large amount of slow memory is constantly updated by the fast memory, giving the appearance of a large fast memory array. A common implementation of the technique is known as a high-speed memory cache. The cache may be thought of as fast acting shock absorber smoothing out the bumps in memory access. When more memory is required than the shock can absorb, it bottoms out and slow speed memory is accessed. Most memory operations can be handled by the shock absorber itself.

The microprocessor 50 architecture has the ALU 80 (FIG. 2) directly coupled to the top two stack locations 76 and 78. The access time of the stack 74 therefore directly affects the execution speed of the processor. The microprocessor 50 stack architecture is particularly suitable to a triple cache technique, shown in FIG. 21 which offers the appearance of a large stack memory operating at the speed of on-chip latches 450. Latches 450 are the fastest form of memory device built on the chip, delivering data in as little as 3 nsec. However latches 450 require large numbers of transistors to construct. On-chip RAM 452 requires fewer transistors than latches, but is slower by a factor of five (15 nsec access). Off-chip RAM 150 is the slowest storage of all. The microprocessor 50 organizes the stack memory hierarchy as three interconnected stacks 450, 452 and 454. The latch stack 450 is the fastest and most frequently used. The on-chip RAM stack 452 is next. The off-chip RAM stack 454 is slowest. The stack modulation determines the effective access time of the stack. If a group of stack operations never push or pull more than four consecutive items on the stack, operations will be entirely performed in the 3 nsec latch stack. When the four latches 456 are filled, the data in the bottom of the latch stack 450 is written to the top of the on-chip RAM stack 452. When the sixteen locations 458 in the on-chip RAM stack 452 are filled, the data in the bottom of the on-chip RAM stack 452 is written to the top of the off-chip RAM stack 454. When popping data off a full stack 450, four pops will be performed before stack empty line 460 from the latch stack pointer 462 transfers data from the on-chip RAM stack 452. By waiting for the latch stack 450 to empty before performing the slower on-chip RAM access the high effective speed of the latches 456 are made available to the processor. The same approach is employed with the on-chip RAM stack 452 and the off-chip RAM stack 454.

POLYNOMIAL GENERATION INSTRUCTION

Polynomials are useful for error correction, encryption, data compression, and fractal generation. A polynomial is generated by a sequence of shift and exclusive OR operations. Special chips are provided for this purpose in the prior art.

The microprocessor 50 is able to generate polynomials at high speed without external hardware by slightly modifying how the ALU 80 works. As shown in FIG. 21, a polynomial is generated by loading the "order" (also known as the feedback terms) into C Register 470. The value thirty one (resulting in 32 iterations) is loaded into DOWN COUNTER 472. A register 474 is loaded with zero. B register 476 is loaded with the starting polynomial value. When the POLY

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instruction executes, C register 470 is exclusively ORed with A register 474 if the least significant bit of B register 476 is a one. Otherwise, the contents of the A register 474 passes through the ALU 80 unaltered. The combination of A and B is then shifted right (divided by 2) with shifters 478 and 480. The operation automatically repeats the specified number of iterations, and the resulting polynomial is left in A register 474.

FAST MULTIPLY

Most microprocessors offer a 16x16 or 32x32 bit multiply instruction. Multiply when performed sequentially takes one shift/add per bit or 32 cycles for 32 bit data. The microprocessor 50 provides a high speed multiply which allows multiplication by small numbers using only a small number of cycles. FIG 23 shows the logic used to implement the high speed algorithm. To perform a multiply, the size of the multiplier less one is placed in the DOWN COUNTER 472. For a four bit multiplier, the number three would be stored in the DOWN COUNTER 472. Zero is loaded into the A register 474. The multiplier is written bit reversed into the B Register 476. For example, a bit reversed five (binary 0101) would be written into B as 1010. The multiplicand is written into the C register 470. Executing the FAST MULT instruction will leave the result in the A Register 474, when the count has been completed. The fast multiply instruction is important because many applications scale one number by a much smaller number. The difference in speed between multiplying a 32x32 bit and a 32x4 bit is a factor of 8. If the least significant bit of the multiplier is a "ONE", the contents of the A register 474 and the C register 470 are added. If the least significant bit of the multiplier is a "ZERO", the contents of the A register are passed through the ALU 80 unaltered. The output of the ALU 80 is shifted left by shifter 482 in each iteration. The contents of the B register 476 are shifted right by the shifter 480 in each iteration.

INSTRUCTION EXECUTION PHILOSOPHY

The microprocessor 50 uses high speed D latches in most of the speed critical areas. Slower on-chip RAM is used as secondary storage.

The microprocessor 50 philosophy of instruction execution is to create a hierarchy of speed as follows:

Logic and D latch transfers	1 cycle	20 nsec
Math	2 cycles	40 nsec
Fetch/store on-chip RAM	2 cycles	40 nsec
Fetch/store in current RAS page	4 cycles	80 nsec
Fetch/store with RAS cycle	11 cycles	220 nsec

With a 50 MHZ clock, many operations can be performed in 20 nsec and almost everything else in 40 nsec.

To maximize speed, certain techniques in processor design have been used. They include:

- Eliminating arithmetic operations on addresses,
- Fetching up to four instructions per memory cycle,
- Pipelineless instruction decoding
- Generating results before they are needed,
- Use of three level stack caching

PIPELINE PHILOSOPHY

Computer instructions are usually broken down into sequential pieces, for example: fetch, decode, register read, execute, and store. Each piece will require a single machine cycle. In most Reduced Instruction Set Computer (RISC) chips, instruction require from three to six cycles.

RISC instructions are very parallel. For example, each of 70 different instructions in the SPARC (SUN Computer's RISC chip) has five cycles. Using a technique called

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'pipelining', the different phases of consecutive instructions can be overlapped.

To understand pipelining think of building five residential homes. Each home will require in sequence, a foundation, framing, plumbing and wiring, roofing, and interior finish. Assume that each activity takes one week. To build one house will take five weeks.

But what if you want to build an entire subdivision? You have only one of each work crew, but when the foundation men finish on the first house, you immediately start them on the second one, and so on. At the end of five weeks, the first home is complete, but you also have five foundations. If you have kept the framing, plumbing, roofing, and interior guys all busy, from five weeks on a new house will be completed each week.

This is the way a RISC chip like SPARC appears to execute an instruction in a single machine cycle. In reality, a RISC chip is executing one fifth of five instructions each machine cycle. And if five instructions stay in sequence, an instruction will be completed each machine cycle.

The problems with a pipeline are keeping the pipe full with instructions. Each time an out of sequence instruction such as a BRANCH or CALL occurs, the pipe must be refilled with the next sequence. The resulting dead time to refill the pipeline can become substantial when many IF/THEN/ELSE statements or subroutines are encountered.

THE PIPELINE APPROACH

The microprocessor 50 has no pipeline as such. The approach of this microprocessor to speed is to overlap instruction fetching with execution of the previously fetched instruction(s). Beyond that, over half the instructions (the most common ones) execute entirely in a single machine cycle of 20 nsec. This is possible because:

1. Instruction decoding resolves in 2.5 nsec.
2. Incremented/decremented and some math values are calculated before they are needed, requiring only a latching signal to execute.
3. Slower memory is hidden from high speed operations by high-speed D latches which access in 4 nsec.

The disadvantage for this microprocessor is a more complex chip design process. The advantage for the chip user is faster ultimate throughput since pipeline stalls cannot exist. Pipeline synchronization with availability flag bits and other such pipeline handling is not required by this microprocessor.

For example, in some RISC machines an instruction which tests a status flag may have to wait for up to four cycles for the flag set by the previous instruction to be available to be tested. Hardware and software debugging is also somewhat easier because the user doesn't have to visualize five instructions simultaneously in the pipe.

OVERLAPPING INSTRUCTION FETCH/EXECUTE

The slowest procedure the microprocessor 50 performs is to access memory. Memory is accessed when data is read or written. Memory is also read when instructions are fetched. The microprocessor 50 is able to hide fetch of the next instruction behind the execution of the previously fetched instruction(s). The microprocessor 50 fetches instructions in 4-byte instruction groups. An instruction group may contain from one to four instructions. The amount of time required to execute the instruction group ranges from 4 cycles for simple instructions to 64 cycles for a multiply.

When a new instruction group is fetched, the microprocessor instruction decoder looks at the most significant bit of all four of the bytes. The most significant bit of an instruction determines if a memory access is required. For example, CALL, FETCH, and STORE all require a memory access to

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execute. If all four bytes have nonzero most significant bits, the microprocessor initiates the memory fetch of the next sequential 4-byte instruction group. When the last instruction in the group finishes executing, the next 4-byte instruction group is ready and waiting on the data bus needing only to be latched into the instruction register. If the 4-byte instruction group required four or more cycles to execute and the next sequential access was a column address strobe (CAS) cycle, the instruction fetch was completely overlapped with execution.

INTERNAL ARCHITECTURE

The microprocessor 50 architecture consists of the following:

PARAMETER STACK	Y REGISTER
ALU*	RETURN STACK
←---32 BITS---→	←---32 BITS---→
16 DEEP	16 DEEP
Used for math and logic	Used for subroutine and interrupt return addresses as well as local variables.
Push down stack	Push down stack
Can overflow into off-chip RAM	Can overflow into off-chip RAM
	Can also be accessed relative to top of stack.
LOOP COUNTER	(32-bits, can decrement by 1)
	Used by class of test and loop instructions
X REGISTER	(32-bits, can increment or decrement by 4). Used to point to RAM locations
PROGRAM COUNTER	(32-bits, increments by 4). Points to 4-byte instruction groups in RAM
INSTRUCTION REG	(32-Bits) Holds 4-byte instruction groups while they are being decoded and executed.
MODE - A register with mode and status bits	
MODE-BITS:	
- Slow down memory accesses by 8 if "1". Run full speed if "0" (Provided for access to slow EPROM)	
- Divide the system clock by 1023 if "1" to reduce power consumption. Run full speed if "0" (On-chip counters slow down if this bit is set)	
- Enable external interrupt 1	
- Enable external interrupt 2	
- Enable external interrupt 3	
- Enable external interrupt 4	
- Enable external interrupt 5	
- Enable external interrupt 6	
- Enable external interrupt 7	
ON-CHIP MEMORY LOCATIONS:	
MODE-BITS	
DMA-POINTER	
DMA-COUNTER	
STACK-POINTER	- Pointer into Parameter Stack.
STACK-DEPTH	- Depth of on-chip Parameter Stack
RSTACK-POINTER	- Pointer into Return Stack
RSTACK-DEPTH	- Depth of on-chip Return Stack

*Math and logic operations use the TOP item and NEXT to top Parameter Stack items as the operands. The result is pushed onto the Parameter Stack.
*Return addresses from subroutines are placed on the Return Stack. The Y REGISTER is used as a pointer to RAM locations. Since the Y REGISTER is the top item of the Return Stack, nesting of indices is straightforward.

ADDRESSING MODE HIGH POINTS

The data bus is 32-bits wide. All memory fetches and stores are 32-bits. Memory bus addresses are 30 bits. The least significant 2 bits are used to select one-of-four bytes in some addressing modes. The Program Counter, X Register, and Y Register are implemented as D latches with their outputs going to the memory address bus and the bus incrementer/decrementer. Incrementing one of these registers can happen quickly, because the incremented value has already rippled through the inc/dec logic and need only be

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clocked into the latch. Branches and Calls are made to 32-bit word boundaries.

INSTRUCTION SET

32-BIT INSTRUCTION FORMAT

The thirty two bit instructions are CALL, BRANCH, BRANCH-IF-ZERO, and LOOP-IF-NOT-DONE. These instructions require the calculation of an effective address. In many computers, the effective address is calculated by adding or subtracting an operand with the current Program Counter. This math operation requires from four to seven machine cycles to perform and can definitely bog down machine execution. The microprocessor's strategy is to perform the required math operation at assembly or linking time and do a much simpler "Increment to next page" or "Decrement to previous page" operation at run time. As a result, the microprocessor branches execute in a single cycle.

24-BIT OPERAND FORM:

Byte 1 Byte 2 Byte 3 Byte 4
WWWWWW XX-YYYYYYY-YYYYYYY-YYYYYYY

With a 24-bit operand, the current page is considered to be defined by the most significant 6 bits of the Program Counter.

16-BIT OPERAND FORM: QQQQQQQQ-WWWWWW
XX-YYYYYYY-YYYYYYY With a 16-bit operand, the current page is considered to be defined by the most significant 14 bits of the Program Counter.

8-BIT OPERAND FORM: QQQQQQQQ-QQQQQQQQ-
WWWWWW XX-YYYYYYY With an 8-bit operand, the current page is considered to be defined by the most significant 22 bits of the Program Counter.

QQQQQQQQ—Any 8-bit instruction

WWWWWW—Instruction op-code

XX—Select how the address bits will be used:

00—Make all high-order bits zero (Page zero addressing)

01—Increment the high-order bits (Use next page)

10—Decrement the high-order bits (Use previous page)

11—Leave the high-order bits unchanged (Use current page)

YYYYYYY—The address operand field. This field is always shifted left two bits (to generate a word rather than byte address) and loaded into the Program Counter. The microprocessor instruction decoder figures out the width of the operand field by the location of the instruction op-code in the four bytes.

The compiler or assembler will normally use the shortest operand required to reach the desired address so that the leading bytes can be used to hold other instructions. The effective address is calculated by combining:

The current Program Counter.

The 8, 16, or 24 bit address operand in the instruction, Using one of the four allowed addressing modes.

EXAMPLES OF EFFECTIVE ADDRESS CALCULATION

Example 1

Byte 1 Byte 2 Byte 3 Byte 4
QQQQQQQ QQQQQQQ 00000011 10011000

The "QQQQQQQs" in Byte 1 and 2 indicate space in the 4-byte memory fetch which could be hold two other

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instructions to be executed prior to the CALL instruction. Byte 3 indicates a CALL instruction (six zeros) in the current page (indicated by the 11 bits). Byte 4 indicates that the hexadecimal number 98 will be forced into the Program Counter bits 2 through 10. (Remember, a CALL or BRANCH always goes to a word boundary so the two least significant bits are always set to zero). The effect of this instruction would be to CALL a subroutine at WORD location HEX 98 in the current page. The most significant 22 bits of the Program Counter define the current page and will be unchanged.

Example 2

Byte 1	Byte 2	Byte 3	Byte 4
00000101	00000001	00000000	00000000

If we assume that the Program Counter was HEX 0000 0156 which is binary:

00000000 00000000 00000001 01010110=OLD PROGRAM COUNTER

Byte 1 indicates a BRANCH instruction op code (000001) and "01" indicates select the next page. Byte 2, 3, and 4 are the address operand. These 24-bits will be shifted to the left two places to define a WORD address. HEX 0156 shifted left two places is HEX 0558. Since this is a 24-bit operand instruction, the most significant 6 bits of the Program Counter define the current page. These six bits will be incremented to select the next page. Executing this instruction will cause the Program Counter to be loaded with HEX 0400 0558 which is binary:

00000100 00000000 00000101 01011000=NEW PROGRAM COUNTER
INSTRUCTIONS
CALL-LONG

0000 00XX-YYYYYYYY-YYYYYYYY-YYYYYYYY
Load the Program Counter with the effective WORD address specified. Push the current PC contents onto the RETURN STACK.

OTHER EFFECTS: CARRY or modes, no effect. May cause Return Stack to force an external memory cycle if on-chip Return Stack is full.
BRANCH

0000 01XX-YYYYYYYY-YYYYYYYY-YYYYYYYY
Load the Program Counter with the effective WORD address specified.

OTHER EFFECTS: NONE
BRANCH-IF-ZERO

0000 10XX-YYYYYYYY-YYYYYYYY-YYYYYYYY
Test the TOP value on the Parameter Stack. If the value is equal to zero, load the Program Counter with the effective WORD address specified. If the TOP value is not equal to zero, increment the Program Counter and fetch and execute the next instruction.

OTHER EFFECTS: NONE
LOOP-IF-NOT-DONE

0000 11YY-(XXXX XXXX)-(XXXX XXXX)-(XXXX XXXX)

If the LOOP COUNTER is not zero, load the Program Counter with the effective WORD address specified. If the LOOP COUNTER is zero, decrement the LOOP COUNTER, increment the Program Counter and fetch and execute the next instruction.

OTHER EFFECTS: NONE
8-BIT INSTRUCTIONS PHILOSOPHY

Most of the work in the microprocessor 50 is done by the 8-bit instructions. Eight bit instructions are possible with the

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microprocessor because of the extensive use of implied stack addressing. Many 32-bit architectures use 8-bits to specify the operation to perform but use an additional 24-bits to specify two sources and a destination.

For math and logic operations, the microprocessor 50 exploits the inherent advantage of a stack by designating the source operand(s) as the top stack item and the next stack item. The math or logic operation is performed, the operands are popped from the stack, and the result is pushed back on the stack. The result is a very efficient utilization of instruction bits as well as registers. A comparable situation exists between Hewlett Packard calculators (which use a stack) and Texas Instrument calculators which don't. The identical operation on an HP will require one half to one third the keystrokes of the TI.

The availability of 8-bit instructions also allows another architectural innovation, the fetching of four instructions in a single 32-bit memory cycle. The advantages of fetching multiple instructions are:

Increased execution speed even with slow memories,
Similar performance to the Harvard (separate data and instruction busses) without the expense,

Opportunities to optimize groups of instructions,
The capability to perform loops within this mini-cache.

The microloops inside the four instruction group are effective for searches and block moves.

SKIP INSTRUCTIONS

The microprocessor 50 fetches instructions in 32-bit chunks called 4-byte instruction groups. These four bytes may contain four 8-bit instructions or some mix of 8-bit and 16 or 24-bit instructions. SKIP instructions in the microprocessor skip any remaining instructions in a 4-byte instruction group and cause a memory fetch to get the next 4-byte instruction group. Conditional SKIPS when combined with 3-byte BRANCHES will create conditional BRANCHES. SKIPS may also be used in situations when no use can be made of the remaining bytes in a 4-instruction group. A SKIP executes in a single cycle, whereas a group of three NOPs would take three cycles.

SKIP-ALWAYS—Skip any remaining instructions in this 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group.

SKIP-IF-ZERO—If the TOP item of the Parameter Stack is zero, skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the TOP item is not zero, execute the next sequential instruction.

SKIP-IF-POSITIVE—If the TOP item of the Parameter Stack has a the most significant bit (the sign bit) equal to "0" skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the TOP item is not "0", execute the next sequential instruction.

SKIP-IF-NO-CARRY—If the CARRY flag from a SHIFT or arithmetic operation is not equal to 1, skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the CARRY is equal to 1, execute the next sequential instruction.

SKIP-NEVER (NOP) execute the next sequential instruction. (Delay one machine cycle)

SKIP-IF-NOT-ZERO—If the TOP item on the Parameter Stack is not equal to "0" skip any remaining instructions

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in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the TOP item is equal "0", execute the next sequential instruction.

SKIP-IF-NEGATIVE—If the TOP item on the Parameter Stack has its most significant bit (sign bit) set to "1", skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the TOP item has its most significant bit set to "0", execute the next sequential instruction.

SKIP-IF-CARRY—If the CARRY flag is set to "1" as a result of SHIFT or arithmetic operation, skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the CARRY flag is "0", execute the next sequential instruction.

MICROLOOPS

Microloops are a unique feature of the microprocessor architecture which allows controlled looping within a 4-byte instruction group. A microloop instruction tests the LOOP COUNTER for "0" and may perform an additional test. If the LOOP COUNTER is not "0" and the test is met, instruction execution continues with the first instruction in the 4-byte instruction group, and the LOOP COUNTER is decremented. A microloop instruction will usually be the last byte in a 4-byte instruction group, but it can be any byte. If the LOOP COUNTER is "0" or the test is not met, instruction execution continues with the next instruction. If the microloop is the last byte in the 4-byte instruction group, the most significant 30-bits of the Program Counter are incremented and the next 4-byte instruction group is fetched from memory. On a termination of the loop on LOOP COUNTER equal to "0", the LOOP COUNTER will remain at "0". Microloops allow short iterative work such as moves and searches to be performed without slowing down to fetch instructions from memory.

EXAMPLE

Byte 1 FETCH-VIA-X-AUTO-INCREMENT	Byte 2 STORE-VIA-Y-AUTOINCREMENT
Byte 3 LOOP-UNTIL-DONE	Byte 4 QQQQQQQQ

This example will perform a block move. To initiate the transfer, X will be loaded with the starting address of the source. Y will be loaded with the starting address of the destination. The LOOP COUNTER will be loaded with the number of 32-bit words to move. The microloop will FETCH and STORE and count down the LOOP COUNTER until it reaches zero. QQQQQQQQ indicates any instruction can follow.

MICROLOOP INSTRUCTIONS

LOOP-UNTIL-DONE—If the LOOP COUNTER is not "0", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0", continue execution with the next instruction.

LOOP-IF-ZERO—If the LOOP COUNTER is not "0" and the TOP item on the Parameter Stack is "0", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the TOP item is "1", continue execution with the next instruction.

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LOOP-IF-POSITIVE—If the LOOP COUNTER is not "0" and the most significant bit (sign bit) is "0", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the TOP item is "1", continue execution with the next instruction.

LOOP-IF-NOT-CARRY-CLEAR—If the LOOP COUNTER is not "0" and the floating point exponents found in TOP and NEXT are not aligned, continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the exponents are aligned, continue execution with the next instruction. This instruction is specifically designed for combination with special SHIFT instructions to align two floating point numbers.

LOOP-NEVER—(DECREMENT-LOOP-COUNTER) Decrement the LOOP COUNTER. Continue execution with the next instruction.

LOOP-IF-NOT-ZERO—If the LOOP COUNTER is not "0" and the TOP item of the Parameter Stack is "0", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the TOP item is "1", continue execution with the next instruction.

LOOP-IF-NEGATIVE—If the LOOP COUNTER is not "0" and the most significant bit (sign bit) of the TOP item of the Parameter Stack is "1", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the most significant bit of the Parameter Stack is "0", continue execution with the next instruction.

LOOP-IF-CARRY-SET—If the LOOP COUNTER is not "0" and the exponents of the floating point numbers found in TOP and NEXT are not aligned, continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the exponents are aligned, continue execution with the next instruction.

RETURN FROM SUBROUTINE OR INTERRUPT

Subroutine calls and interrupt acknowledgements cause a redirection of normal program execution. In both cases, the current Program Counter is pushed onto the Return Stack, so the microprocessor can return to its place in the program after executing the subroutine or interrupt service routine.

NOTE: When a CALL to subroutine or interrupt is acknowledged the Program Counter has already been incremented and is pointing to the 4-byte instruction group following the 4-byte group currently being executed. The instruction decoding logic allows the microprocessor to perform a test and execute a return conditional on the outcome of the test in a single cycle. A RETURN pops an address from the Return Stack and stores it to the Program Counter.

RETURN INSTRUCTIONS

RETURN-ALWAYS—Pop the top item from the Return Stack and transfer it to the Program Counter.

RETURN-IF-ZERO—If the TOP item on the Parameter Stack is "0", pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-IF-POSITIVE—If the most significant bit (sign bit) of the TOP item on the Parameter Stack is a "0", pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-IF-CARRY-CLEAR—If the exponents of the floating point numbers found in TOP and NEXT are not aligned, pop the top item from the Return Stack and

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transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-NEVER (NOP)—Execute the next instruction.

RETURN-IF-NOT-ZERO—If the TOP item on the Parameter Stack is not "0", pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-IF-NEGATIVE—If the most significant bit (sign bit) of the TOP item on the Parameter Stack is a "1", pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-IF-CARRY-SET—If the exponents of the floating point numbers found in TOP and NEXT are aligned, pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

HANDLING MEMORY FROM DYNAMIC RAM

The microprocessor 50, like any RISC type architecture, is optimized to handle as many operations as possible on-chip for maximum speed. External memory operations take from 80 nsec. to 220 nsec. compared with on-chip memory speeds of from 4 nsec. to 30 nsec. There are times when external memory must be accessed.

External memory is accessed using three registers:

X-REGISTER—A 30-bit memory pointer which can be used for memory access and simultaneously incremented or decremented.

Y-REGISTER—A 30-bit memory pointer which can be used for memory access and simultaneously incremented or decremented.

PROGRAM-COUNTER—A 30-bit memory pointer normally used to point to 4-byte instruction groups. External memory may be accessed at addresses relative to the PC. The operands are sometimes called "Immediate" or "Literal" in other computers. When used as memory pointer, the PC is also incremented after each operation.

MEMORY LOAD & STORE INSTRUCTIONS

FETCH-VIA-X—Fetch the 32-bit memory content pointed to by X and push it onto the Parameter Stack. X is unchanged.

FETCH-VIA-Y—Fetch the 32-bit memory content pointed to by Y and push it onto the Parameter Stack. Y is unchanged.

FETCH-VIA-X-AUTOINCREMENT—Fetch the 32-bit memory content pointed to by X and push it onto the Parameter Stack. After fetching, increment the most significant 30 bits of X to point to the next 32-bit word address.

FETCH-VIA-Y-AUTOINCREMENT—Fetch the 32-bit memory content pointed to by Y and push it onto the Parameter Stack. After fetching, increment the most significant 30 bits of Y to point to the next 32-bit word address.

FETCH-VIA-X-AUTODECREMENT—Fetch the 32-bit memory content pointed to by X and push it onto the Parameter Stack. After fetching, decrement the most significant 30 bits of X to point to the previous 32-bit word address.

FETCH-VIA-Y-AUTODECREMENT—Fetch the 32-bit memory content pointed to by Y and push it onto the Parameter Stack. After fetching, decrement the most significant 30 bits of Y to point to the previous 32-bit word address.

STORE-VIA-X—Pop the top item of the Parameter Stack and store it in the memory location pointed to by X. X is unchanged.

STORE-VIA-Y—Pop the top item of the Parameter Stack and store it in the memory location pointed to by Y. Y is unchanged.

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STORE-VIA-X-AUTOINCREMENT—Pop the top item of the Parameter Stack and store it in the memory location pointed to by X. After storing, increment the most significant 30 bits of X to point to the next 32-bit word address.

STORE-VIA-Y-AUTOINCREMENT—Pop the top item of the Parameter Stack and store it in the memory location pointed to by Y. After storing, increment the most significant 30 bits of Y to point to the next 32-bit word address.

STORE-VIA-X-AUTODECREMENT—Pop the top item of the Parameter Stack and store it in the memory location pointed to by X. After storing, decrement the most significant 30 bits of X to point to the previous 32-bit word address.

STORE-VIA-Y-AUTODECREMENT—Pop the top item of the Parameter Stack and store it in the memory location pointed to by Y. After storing, decrement the most significant 30 bits of Y to point to the previous 32-bit word address.

FETCH-VIA-PC—Fetch the 32-bit memory content pointed to by the Program Counter and push it onto the Parameter Stack. After fetching, increment the most significant 30 bits of the Program Counter to point to the next 32-bit word address.

*NOTE: When this instruction executes, the PC is pointing to the memory location following the instruction. The effect is of loading a 32-bit immediate operand. This is an 8-bit instruction and therefore will be combined with other 8-bit instructions in a 4-byte instruction fetch. It is possible to have from one to four **FETCH-VIA-PC** instructions in a 4-byte instruction fetch. The PC increments after each execution of **FETCH-VIA-PC**, so it is possible to push four immediate operands on the stack. The four operands would be the found in the four memory locations following the instruction.

BYTE-FETCH-VIA-X—Fetch the 32-bit memory content pointed to by the most significant 30 bits of X. Using the two least significant bits of X, select one of four bytes from the 32-bit memory fetch, right justify the byte in a 32-bit field and push the selected byte preceded by leading zeros onto the Parameter Stack.

BYTE-STORE-VIA-X—Fetch the 32-bit memory content pointed to by the most significant 30 bits of X. Pop the TOP item from the Parameter Stack. Using the two least significant bits of X, place the least significant byte into the 32-bit memory data and write the 32-bit entity back to the location pointed to by the most significant 30 bits of X.

OTHER EFFECTS OF MEMORY ACCESS INSTRUCTIONS:

Any **FETCH** instruction will push a value on the Parameter Stack 74. If the on-chip stack is full, the stack will overflow into off-chip memory stack resulting in an additional memory cycle. Any **STORE** instruction will pop a value from the Parameter Stack 74. If the on-chip stack is empty, a memory cycle will be generated to fetch a value from off-chip memory stack.

HANDLING ON-CHIP VARIABLES

High-level languages often allow the creation of **LOCAL VARIABLES**. These variables are used by a particular procedure and discarded. In cases of nested procedures, layers of these variables must be maintained. On-chip storage is up to five times faster than off-chip RAM, so a means of keeping local variables on-chip can make operations run faster. The microprocessor 50 provides the capability for both on-chip storage of local variables and nesting of multiple levels of variables through the Return Stack.

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The Return Stack 134 is implemented as 16 on-chip RAM locations. The most common use for the Return Stack 134 is storage of return addresses from subroutines and interrupt calls. The microprocessor allows these 16 locations to also be used as addressable registers. The 16 locations may be read and written by two instructions which indicate a Return Stack relative address from 0-15. When high-level procedures are nested, the current procedure variables push the previous procedure variables further down the Return Stack 134. Eventually, the Return Stack will automatically overflow into off-chip RAM.

ON-CHIP VARIABLE INSTRUCTIONS

READ-LOCAL-VARIABLE XXXX—Read the XXXXth location relative to the top of the Return Stack (XXXX is a binary number from 0000-1111). Push the item read onto the Parameter Stack.

OTHER EFFECTS: If the Parameter Stack is full, the push operation will cause a memory cycle to be generated as one item of the stack is automatically stored to external RAM. The logic which selects the location performs a modulo 16 subtraction. If four local variables have been pushed onto the Return Stack, and an instruction attempts to read the fifth item, unknown data will be returned.

WRITE-LOCAL-VARIABLE XXXX—Pop the TOP item of the Parameter Stack and write it into the XXXXth location relative to the top of the Return Stack (XXXX is a binary number from 0000-1111).

OTHER EFFECTS: If the Parameter Stack is empty, the pop operation will cause a memory cycle to be generated to fetch the Parameter Stack item from external RAM. The logic which selects the location performs a modulo 16 subtraction. If four local variables have been pushed onto the Return Stack, and an instruction attempts to write to the fifth item, it is possible to clobber return addresses or wreak other havoc.

REGISTER AND FLIP-FLOP TRANSFER AND PUSH INSTRUCTIONS

DROP—Pop the TOP item from the Parameter Stack and discard it.

SWAP—Exchange the data in the TOP Parameter Stack location with the data in the NEXT Parameter Stack location.

DUP—Duplicate the TOP item on the Parameter Stack and push it onto the Parameter Stack.

PUSH-LOOP-COUNTER—Push the value in LOOP COUNTER onto the Parameter Stack.

POP-RSTACK-PUSH-TO-STACK—Pop the top item from the Return Stack and push it onto the Parameter Stack.

PUSH-X-REG—Push the value in the X Register onto the Parameter Stack.

PUSH-STACK-POINTER—Push the value of the Parameter Stack pointer onto the Parameter Stack.

PUSH-RSTACK-POINTER—Push the value of the Return Stack pointer onto the Return Stack.

PUSH-MODE-BITS—Push the value of the MODE REGISTER onto the Parameter Stack.

PUSH-INPUT—Read the 10 dedicated input bits and push the value (right justified and padded with leading zeros) onto the Parameter Stack.

SET-LOOP-COUNTER—Pop the TOP value from the Parameter Stack and store it into LOOP COUNTER.

POP-STACK-PUSH-TO-RSTACK—Pop the TOP item from the Parameter Stack and push it onto the Return Stack.

SET-X-REG—Pop the TOP item from the Parameter Stack and store it into the X Register.

SET-STACK-POINTER—Pop the TOP item from the Parameter Stack and store it into the Stack Pointer.

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SET-RSTACK-POINTER—Pop the TOP item from the Parameter Stack and store it into the Return Stack Pointer.

SET-MODE-BITS—Pop the TOP value from the Parameter Stack and store it into the MODE BITS.

SET-OUTPUT—Pop the TOP item from the Parameter Stack and output it to the 10 dedicated output bits.

OTHER EFFECTS: Instructions which push or pop the Parameter Stack or Return Stack may cause a memory cycle as the stacks overflow back and forth between on-chip and off-chip memory.

LOADING A SHORT LITERAL

A special case of register transfer instruction is used to push an 8-bit literal onto the Parameter Stack. This instruction requires that the 8-bits to be pushed reside in the last byte of a 4-byte instruction group. The instruction op-code loading the literal may reside in ANY of the other three bytes in the instruction group.

EXAMPLE

BYTE 1	BYTE 2	BYTE 3
LOAD-SHORT-LITERAL	QQQQQQQQ	QQQQQQQQ
BYTE 4	00001111	

In this example, QQQQQQQQ indicates any other 8-bit instruction. When Byte 1 is executed, binary 00001111 (HEX 0F) from Byte 4 will be pushed (right justified and padded by leading zeros) onto the Parameter Stack. Then the instructions in Byte 2 and Byte 3 will execute. The microprocessor instruction decoder knows not to execute Byte 4. It is possible to push three identical 8-bit values as follows:

BYTE 1	BYTE 2
LOAD-SHORT-LITERAL	LOAD-SHORT-LITERAL
BYTE 3	BYTE 4
LOAD-SHORT-LITERAL	00001111
SHORT-LITERAL-INSTRUCTION	

LOAD-SHORT-LITERAL—Push the 8-bit value found in Byte 4 of the current 4-byte instruction group onto the Parameter Stack.

LOGIC INSTRUCTIONS

Logical and math operations used the stack for the source of one or two operands and as the destination for results. The stack organization is a particularly convenient arrangement for evaluating expressions. TOP indicates the top value on the Parameter Stack. NEXT indicates the next to top value on the Parameter Stack.

AND—Pop TOP and NEXT from the Parameter Stack, perform the logical AND operation on these two operands, and push the result onto the Parameter Stack.

OR—Pop TOP and NEXT from the Parameter Stack, perform the logical OR operation on these two operands, and push the result onto the Parameter Stack.

XOR—Pop TOP and NEXT from the Parameter Stack, perform the logical exclusive OR on these two operands, and push the result onto the Parameter Stack.

BIT-CLEAR—Pop TOP and NEXT from the Parameter Stack, toggle all bits in NEXT, perform the logical AND operation on TOP, and push the result onto the Parameter Stack. (Another way of understanding this instruction is thinking of it as clearing all bits in TOP that are set in NEXT.)

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MATH INSTRUCTIONS

Math instruction pop the TOP item and NEXT to top item of the Parameter Stack 74 to use as the operands. The results are pushed back on the Parameter Stack. The CARRY flag is used to latch the "33rd bit" of the ALU result

ADD—Pop the TOP item and NEXT to top item from the Parameter Stack, add the values together and push the result back on the Parameter Stack. The CARRY flag may be changed.

ADD-WITH-CARRY—Pop the TOP item and the NEXT to top item from the Parameter Stack, add the values together. If the CARRY flag is "1" increment the result. Push the ultimate result back on the Parameter Stack. The CARRY flag may be changed.

ADD-X—Pop the TOP item from the Parameter Stack and read the third item from the top of the Parameter Stack. Add the values together and push the result back on the Parameter Stack. The CARRY flag may be changed.

SUB—Pop the TOP item and NEXT to top item from the Parameter Stack, Subtract NEXT from TOP and push the result back on the Parameter Stack. The CARRY flag may be changed.

SUB-WITH-CARRY—Pop the TOP item and NEXT to top item from the Parameter Stack. Subtract NEXT from TOP. If the CARRY flag is "1" increment the result. Push the ultimate result back on the Parameter Stack. The CARRY flag may be changed.

SUB-X—

SIGNED-MULT-STEP—

UNSIGNED-MULT-STEP—

SIGNED-FAST-MULT—

FAST-MULT-STEP—

UNSIGNED-DIV-STEP—

GENERATE-POLYNOMIAL—

ROUND—

COMPARE—Pop the TOP item and NEXT to top item from the Parameter Stack. Subtract NEXT from TOP. If the result has the most significant bit equal to "0" (the result is positive), push the result onto the Parameter Stack. If the result has the most significant bit equal to "1" (the result is negative), push the old value of TOP onto the Parameter Stack. The CARRY flag may be affected.

SHIFT/ROTATE

SHIFT-LEFT—Shift the TOP Parameter Stack item left one bit. The CARRY flag is shifted into the least significant bit of TOP.

SHIFT-RIGHT—Shift the TOP Parameter Stack item right one bit. The least significant bit of TOP is shifted into the CARRY flag. Zero is shifted into the most significant bit of TOP.

DOUBLE-SHIFT-LEFT—Treating the TOP item of the Parameter Stack as the most significant word of a 64-bit number and the NEXT stack item as the least significant word, shift the combined 64-bit entity left one bit. The CARRY flag is shifted into the least significant bit of NEXT.

DOUBLE-SHIFT-RIGHT—Treating the TOP item of the Parameter Stack as the most significant word of a 64-bit number and the NEXT stack item as the least significant word, shift the combined 64-bit entity right one bit. The least significant bit of NEXT is shifted into the CARRY flag. Zero is shifted into the most significant bit of TOP.

OTHER INSTRUCTIONS

FLUSH-STACK—Empty all on-chip Parameter Stack locations into off-chip RAM. (This instruction is useful for multitasking applications). This instruction accesses a counter which holds the depth of the on-chip stack and can require from none to 16 external memory cycles.

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FLUSH-RSTACK—Empty all on-chip Return Stack locations into off-chip RAM. (This instruction is useful for multitasking applications). This instruction accesses a counter which holds the depth of the on-chip Return Stack and can require from none to 16 external memory cycles.

It should further be apparent to those skilled in the art that various changes in form and details of the invention as shown and described may be made. It is intended that such changes be included within the spirit and scope of the claims appended hereto.

What is claimed is:

1. A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.

2. The microprocessor system of claim 1 in which said second clock is a fixed frequency clock.

3. In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:

providing an entire ring oscillator system clock constructed of electronic devices within the integrated circuit, said electronic devices having operating characteristics which will, because said entire ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor;

using the ring oscillator system clock for clocking the microprocessor, said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock;

providing an on chip input/output interface for the microprocessor integrated circuit; and

clocking the input/output interface with a second clock independent of the ring oscillator system clock.

4. The method of claim 3 in which the second clock is a fixed frequency clock.

5. The method of claim 3 further including the step of: transferring information to and from said microprocessor in synchrony with said ring oscillator system clock.

6. A microprocessor system comprising:

a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and

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the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;

an on-chip input/output interface, connected between said said central processing unit and an external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and

an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.

7 The microprocessor system of claim 6 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.

8. The microprocessor system of claim 6 wherein said external clock comprises a fixed-frequency clock which operates synchronously relative to said oscillator.

9. The microprocessor system of claim 6 wherein said oscillator comprises a ring oscillator.

10. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon an integrated circuit substrate, said central processing unit being

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constructed of a first plurality of transistors and being operative at a processing frequency;

providing an entire variable speed clock disposed upon said integrated circuit substrate said variable speed clock being constructed of a second plurality of transistors;

clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;

connecting an on chip input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and

clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.

* * * * *

EXHIBIT C



US005784584A

United States Patent [19]

Moore et al.

[11] Patent Number: **5,784,584**[45] Date of Patent: **Jul. 21, 1998**

[54] **HIGH PERFORMANCE MICROPROCESSOR
USING INSTRUCTIONS THAT OPERATE
WITHIN INSTRUCTION GROUPS**

5 127,091 6/1992 Bonfari et al 395/375

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[57] **ABSTRACT**

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5,440,749

[51] Int. Cl.⁶ **G06F 9/30**

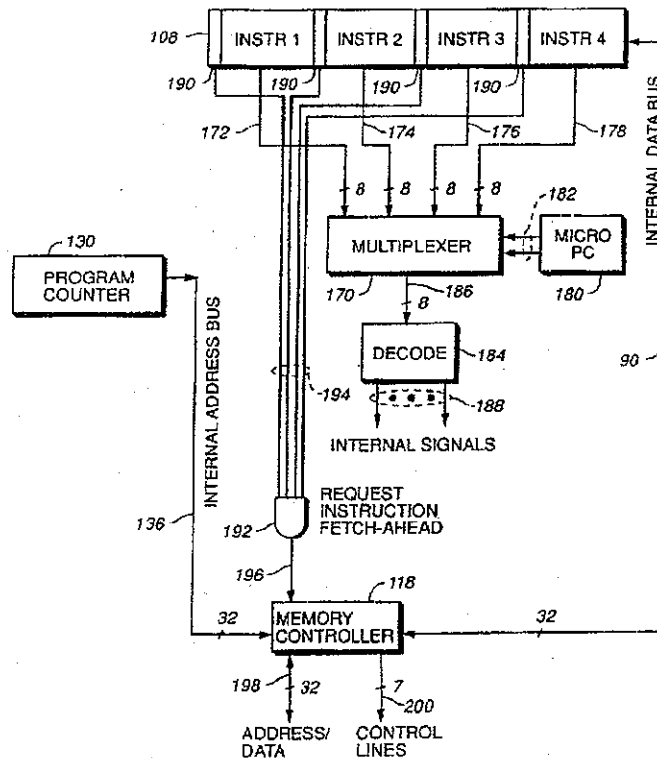
[52] U.S. Cl. **395/376**

[58] Field of Search **395/376, 382,
395/384, 588, 800.23**

A high-performance microprocessor system using instruction that access operands and instructions located relative to the current instruction group rather than located relative to the current instructions, as is the convention is disclosed herein. The microprocessor system includes a central processing unit memory and a bus connecting the central processing unit and memory. An instruction fetching unit, connected to the bus, is provided for fetching instruction groups from the memory for use by the central processing unit and for storage within an instruction register. An instruction supplying unit operates to supply, in succession from the instruction register to the central processing unit, one or more instructions from each of the instruction groups. The system further includes an instruction decoder for configuring the instruction supplying unit to select, from the instruction register, operands associated with instructions from particular instruction groups.

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29 Claims, 19 Drawing Sheets

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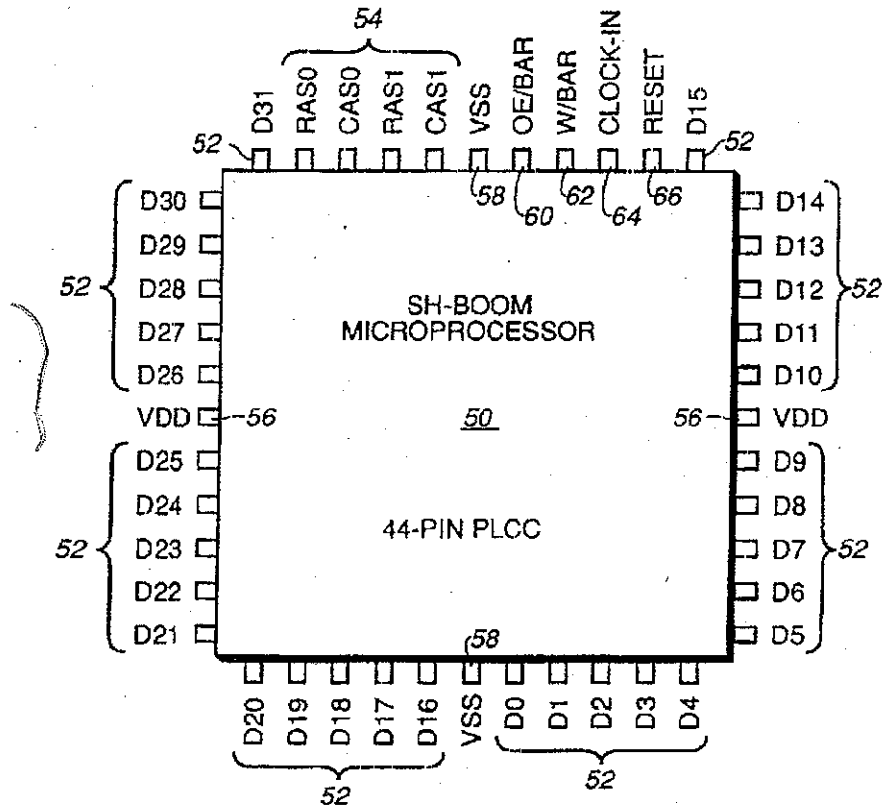


FIG. 1

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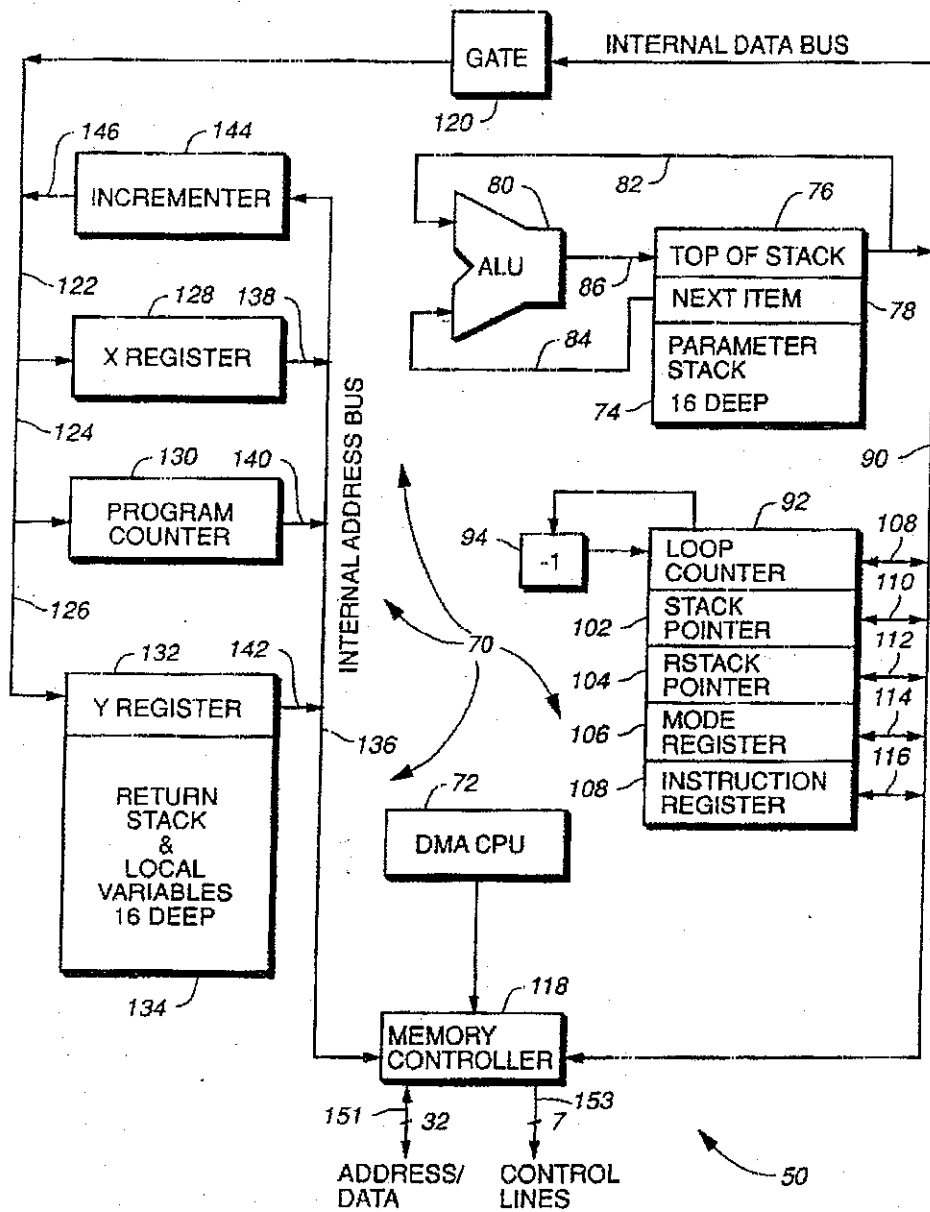


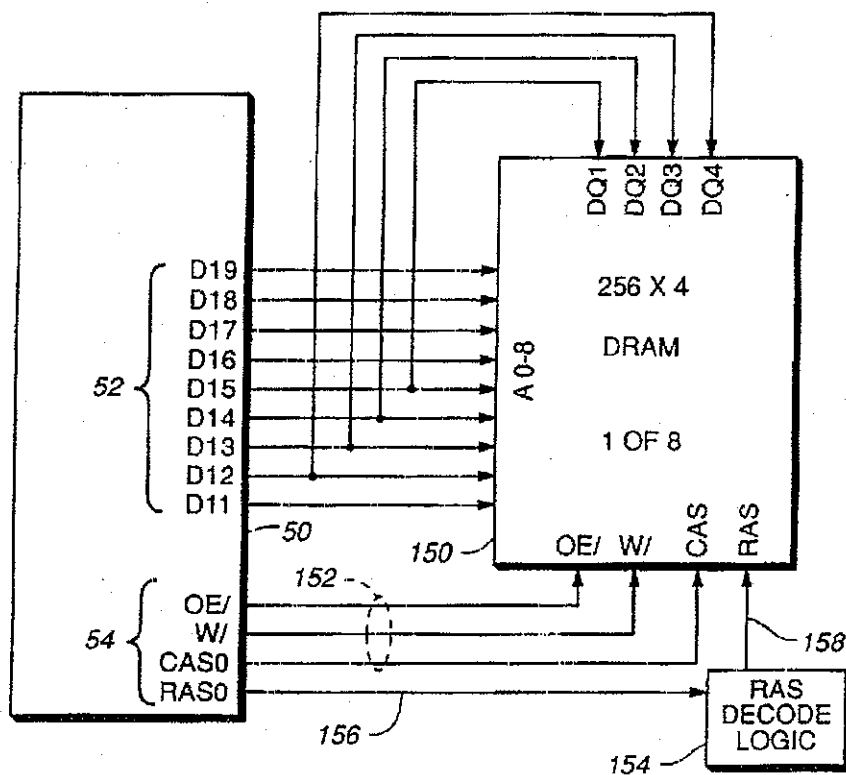
FIG. 2

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**FIG. 3**

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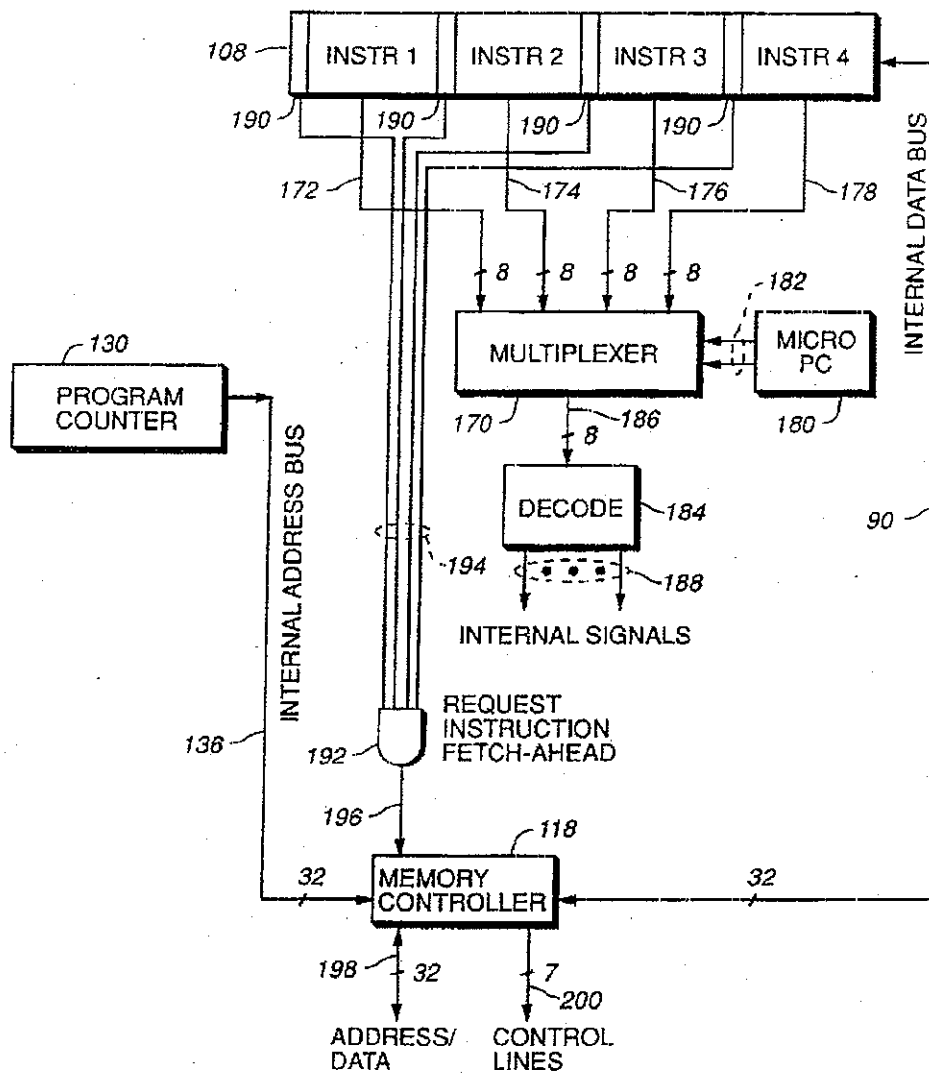


FIG. 4

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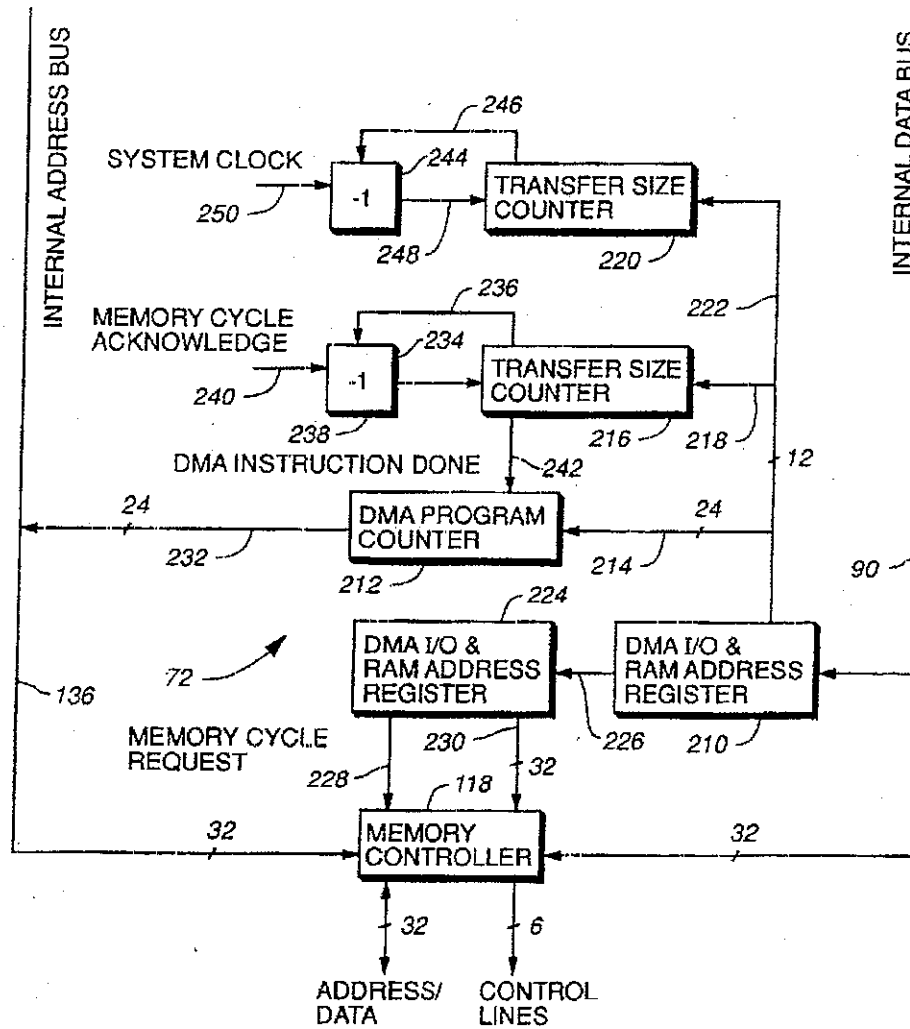


FIG. 5

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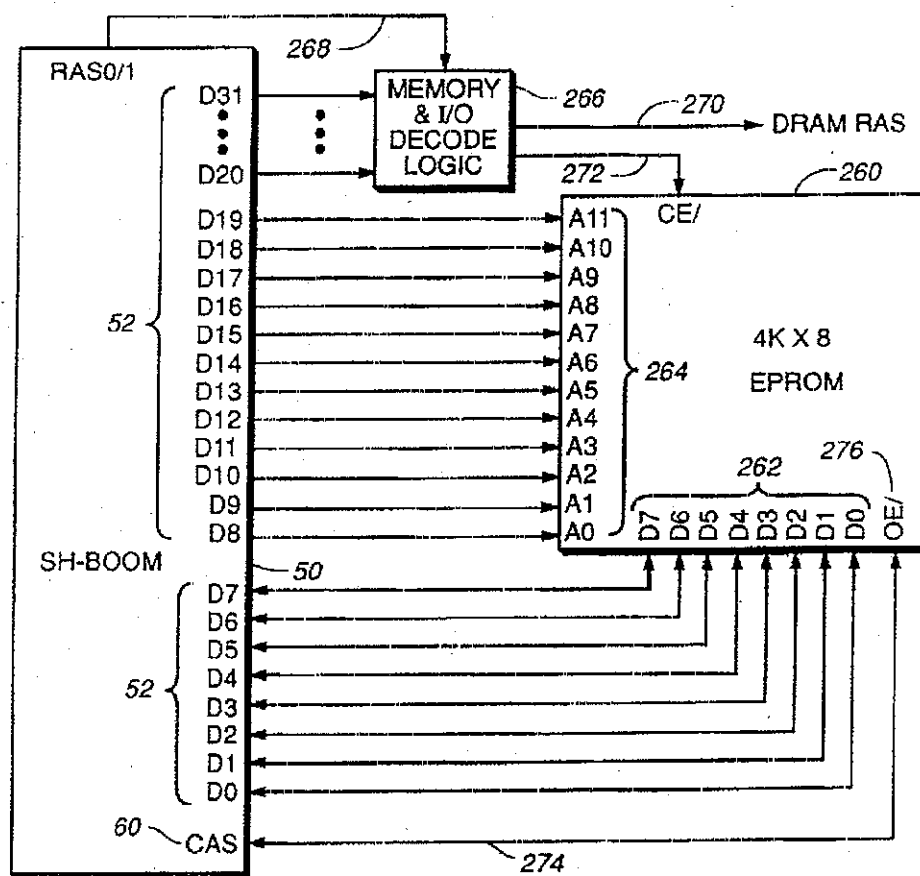


FIG. 6

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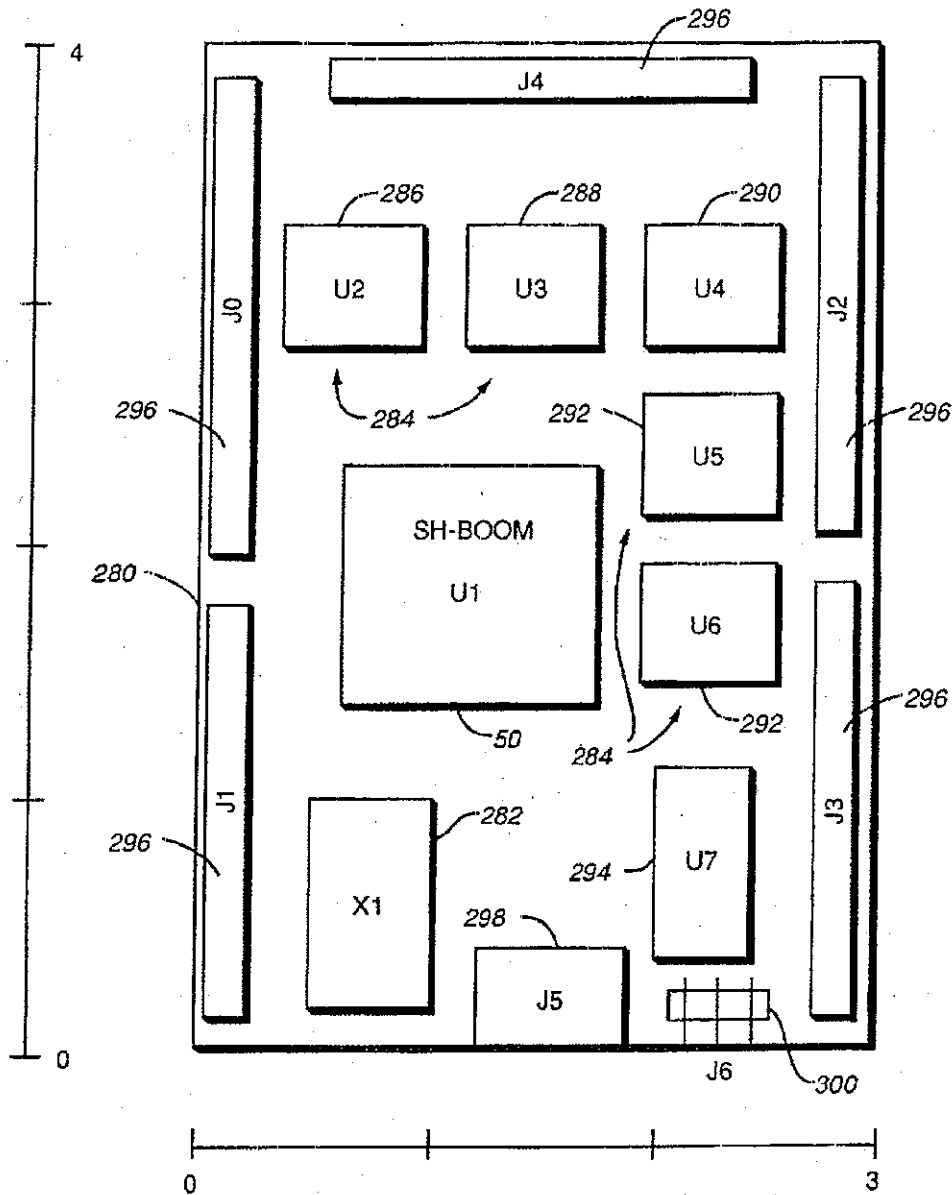


FIG. 7

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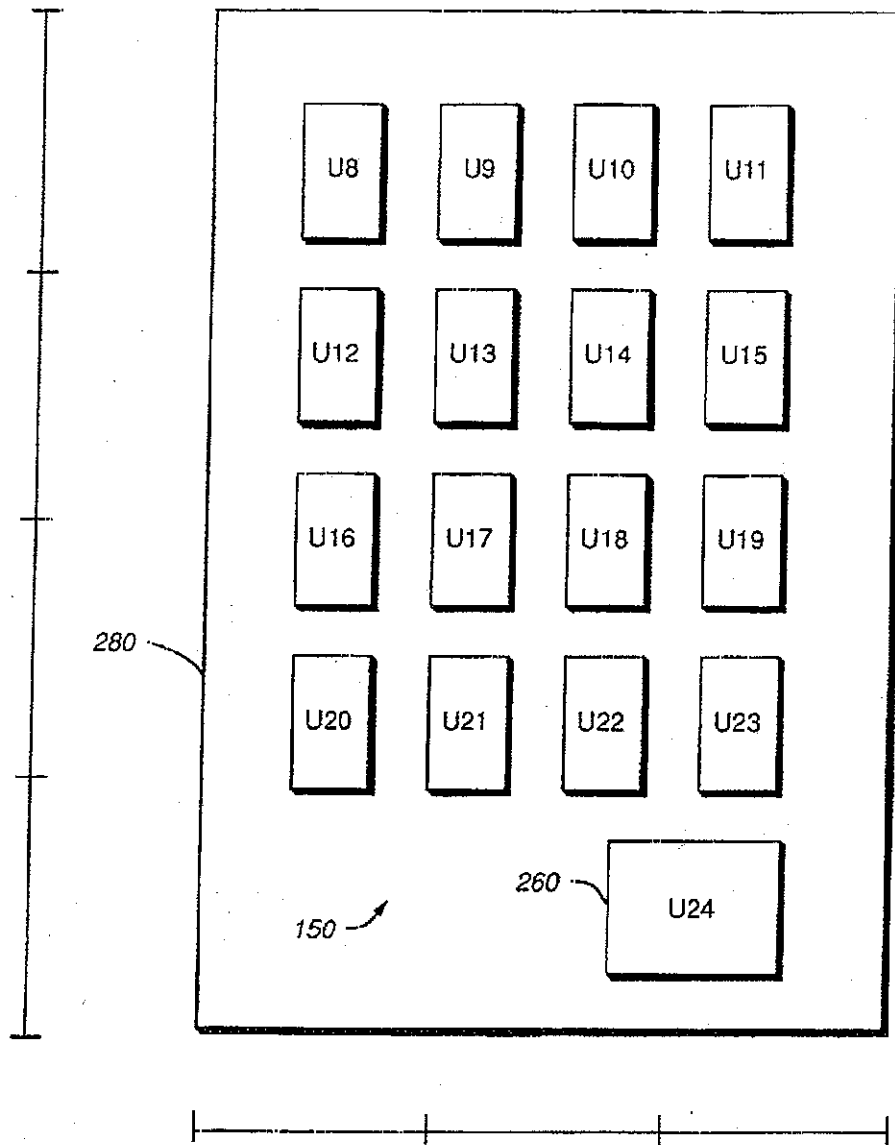


FIG. 8

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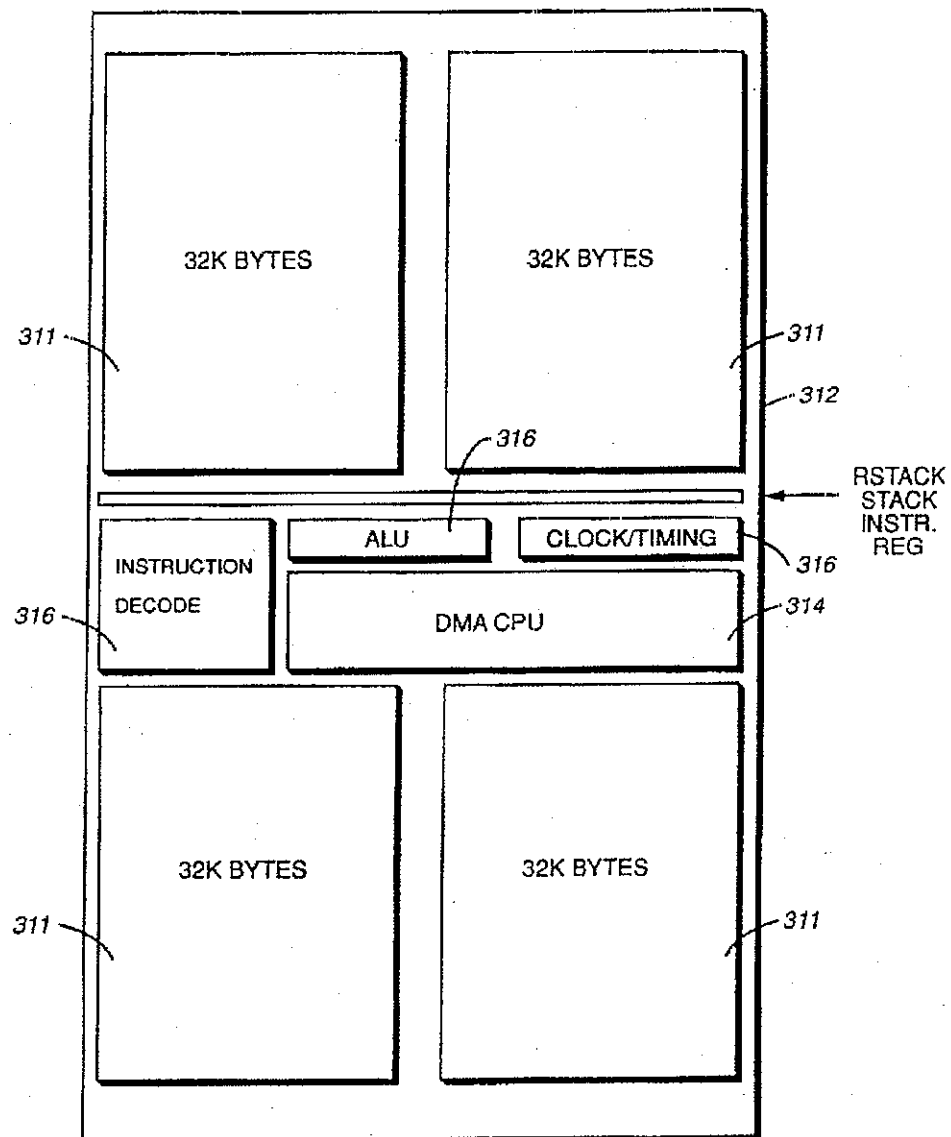


FIG. 9

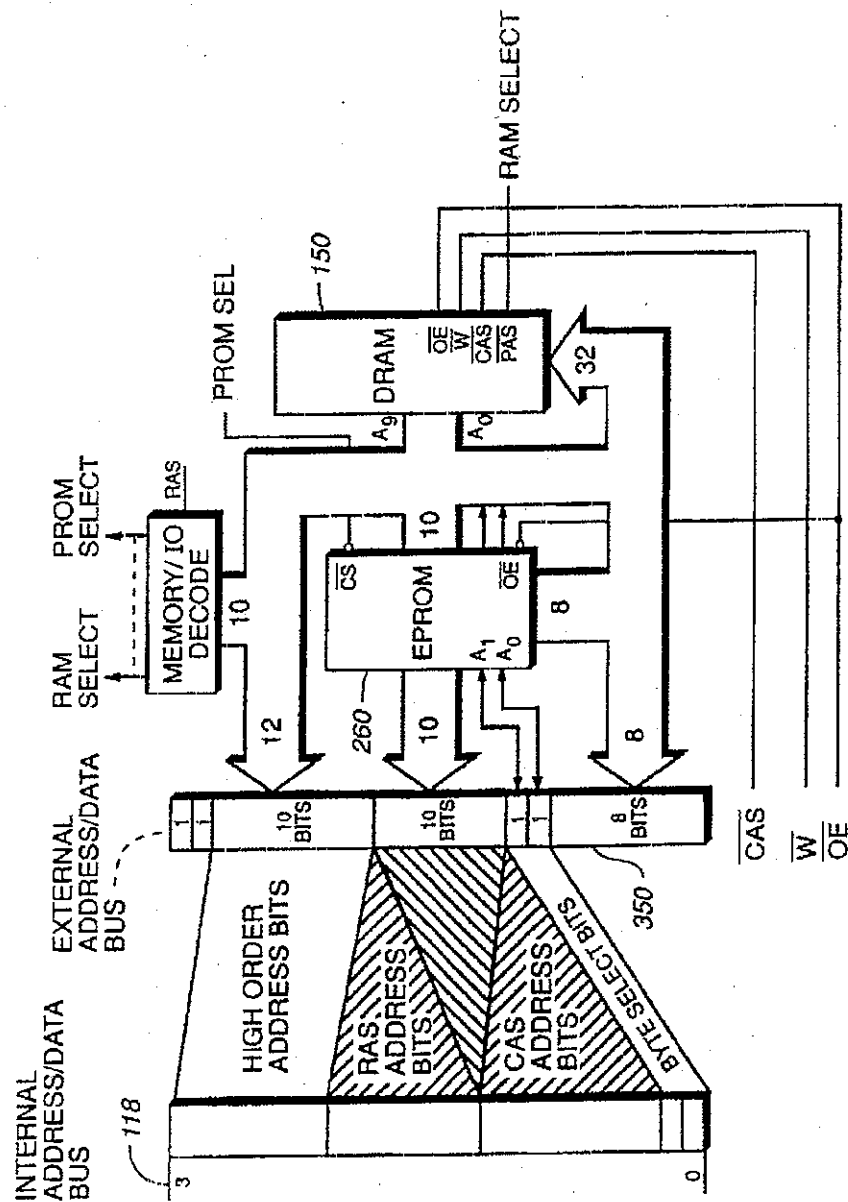


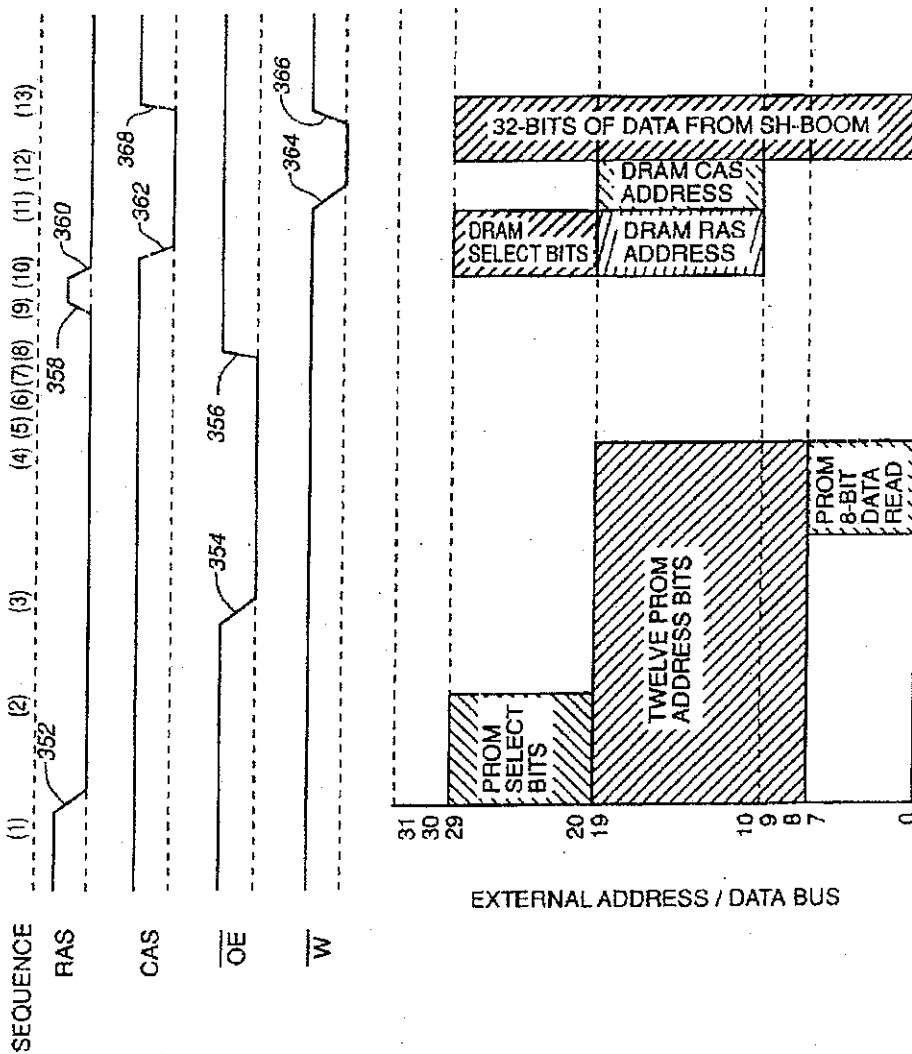
FIG. 10

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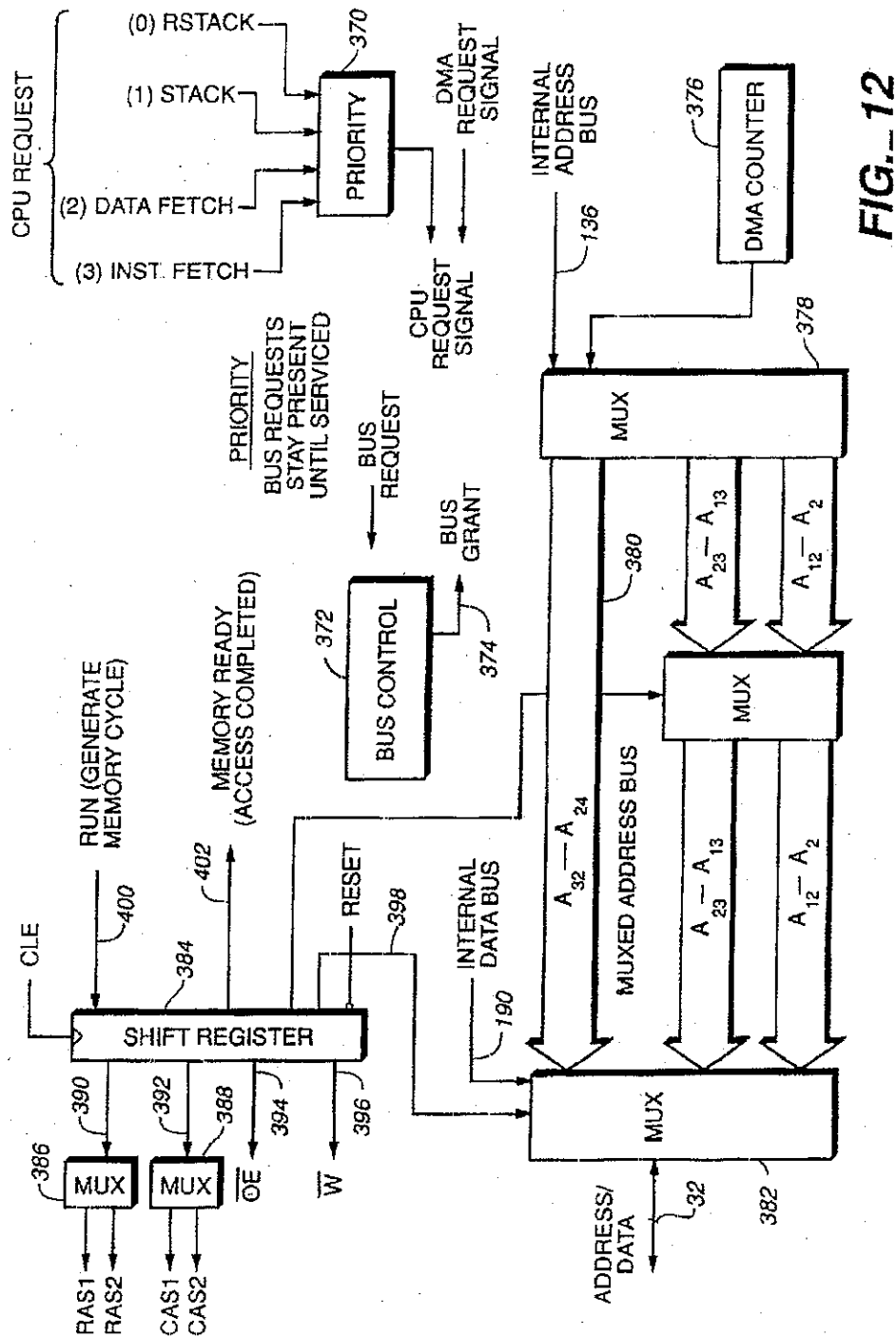


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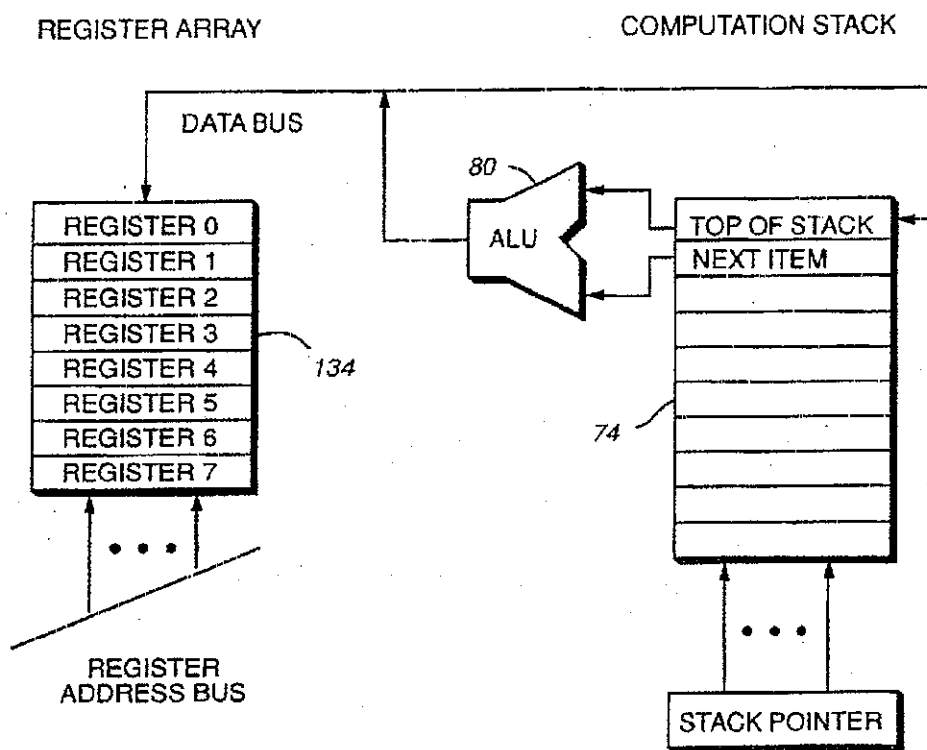


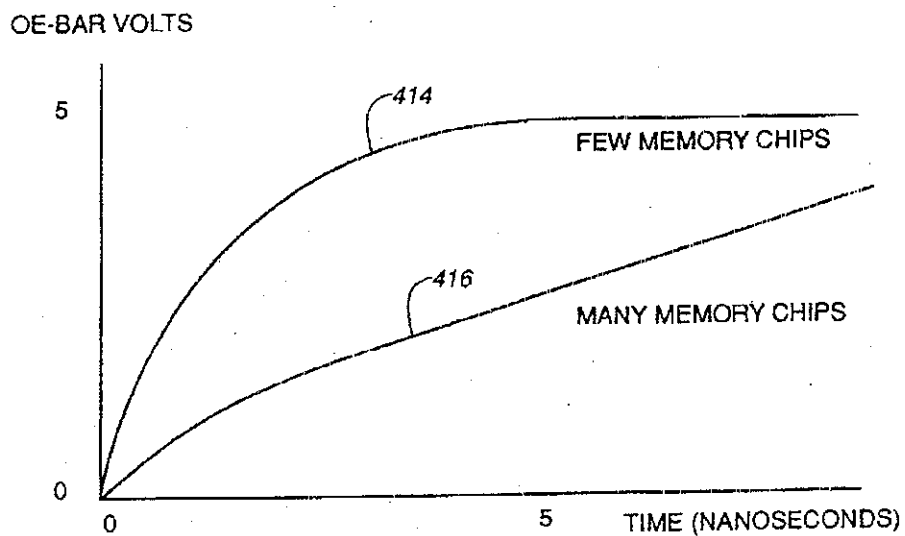
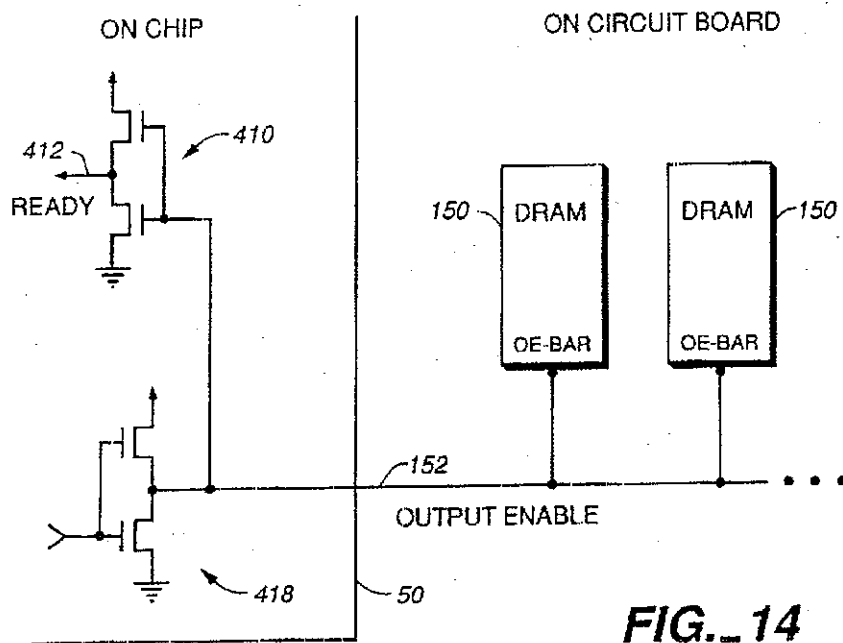
FIG. 13

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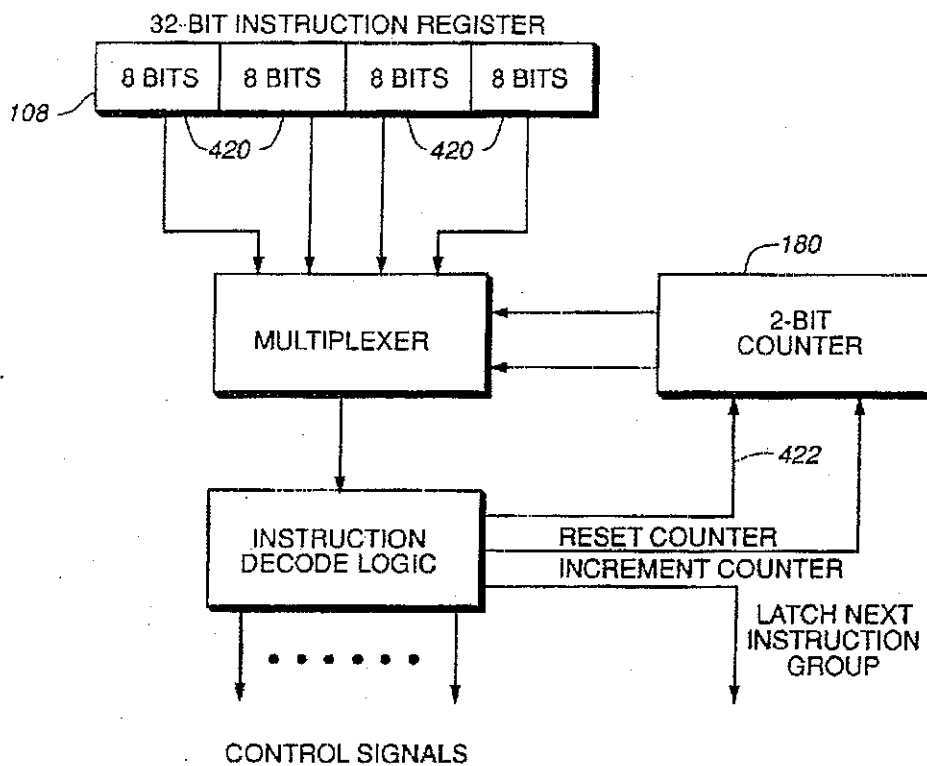
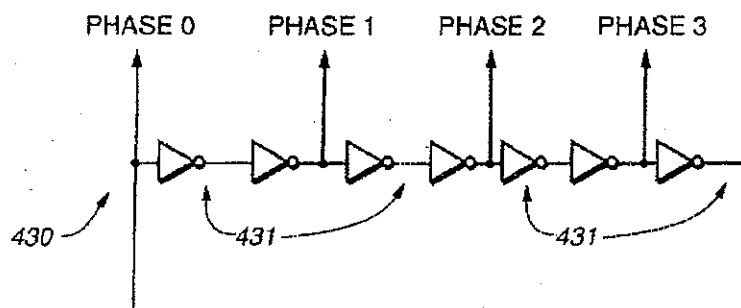


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**FIG. 16****FIG. 18**

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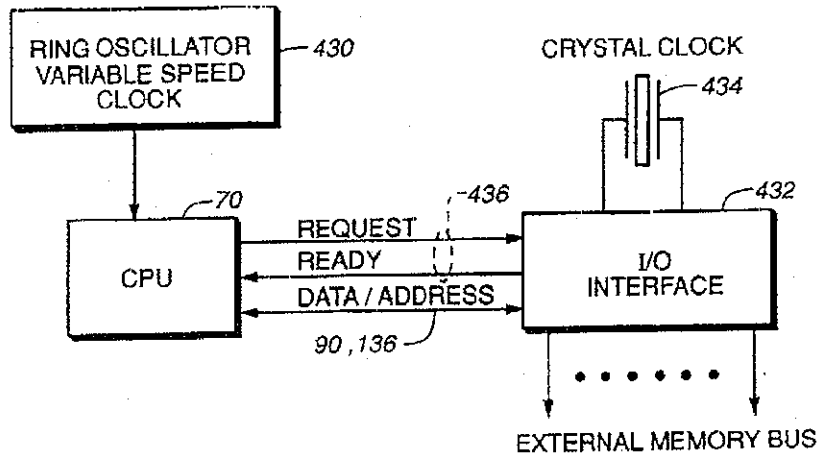


FIG. 17

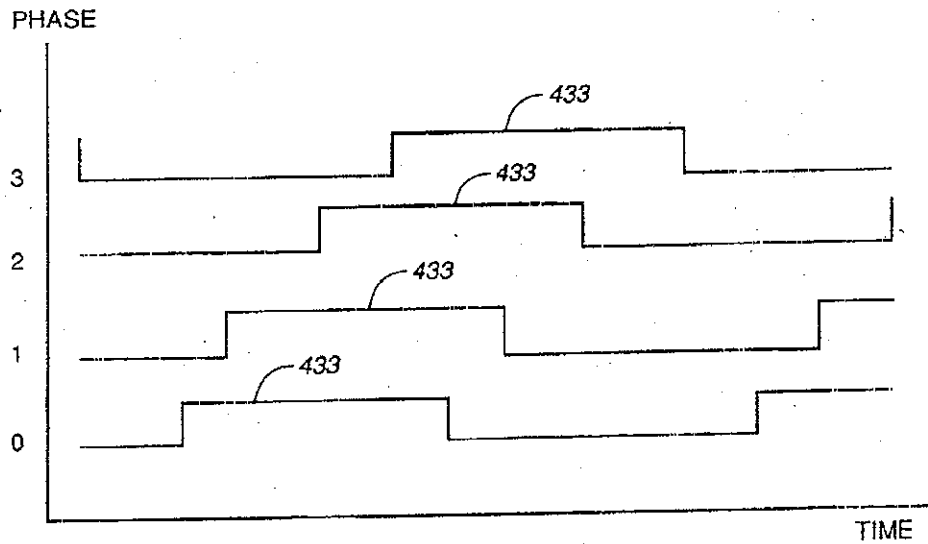


FIG. 19

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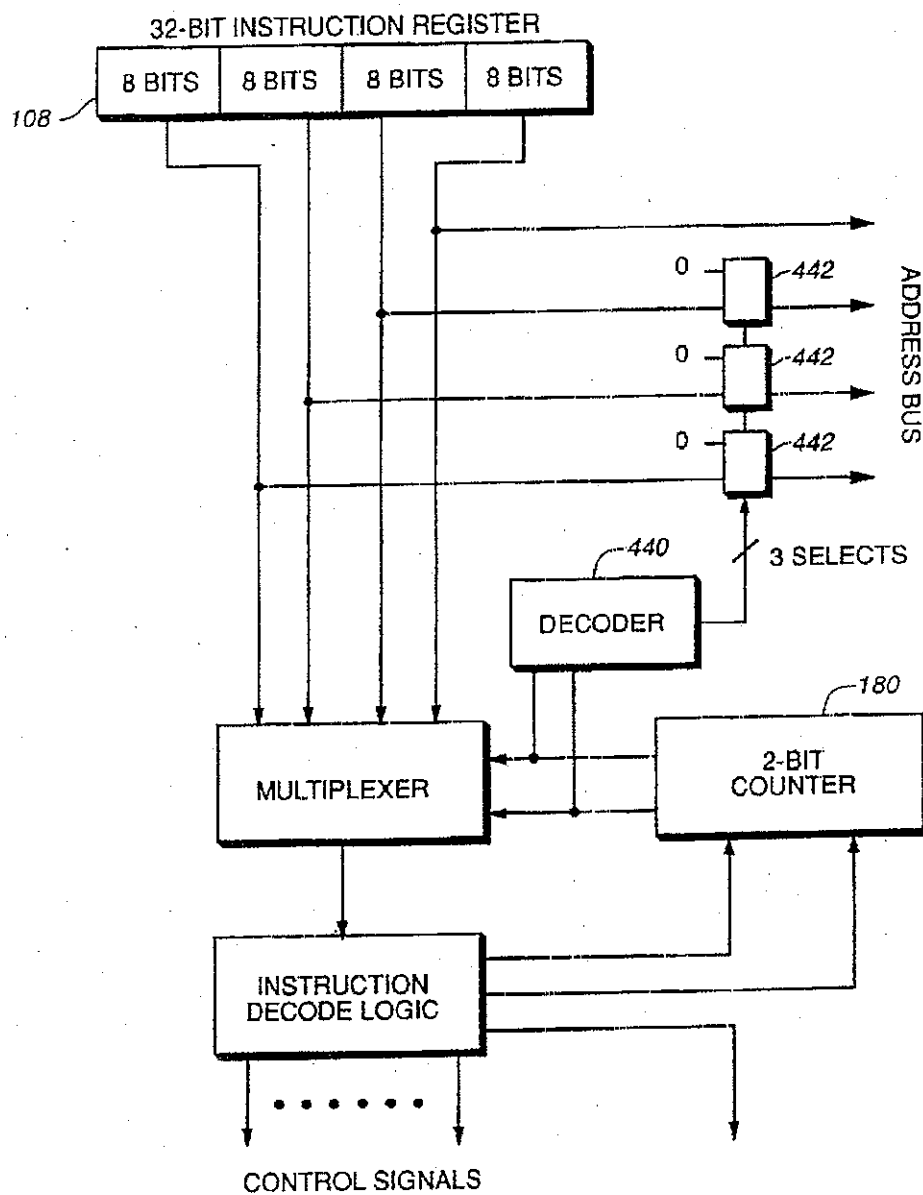


FIG. 20

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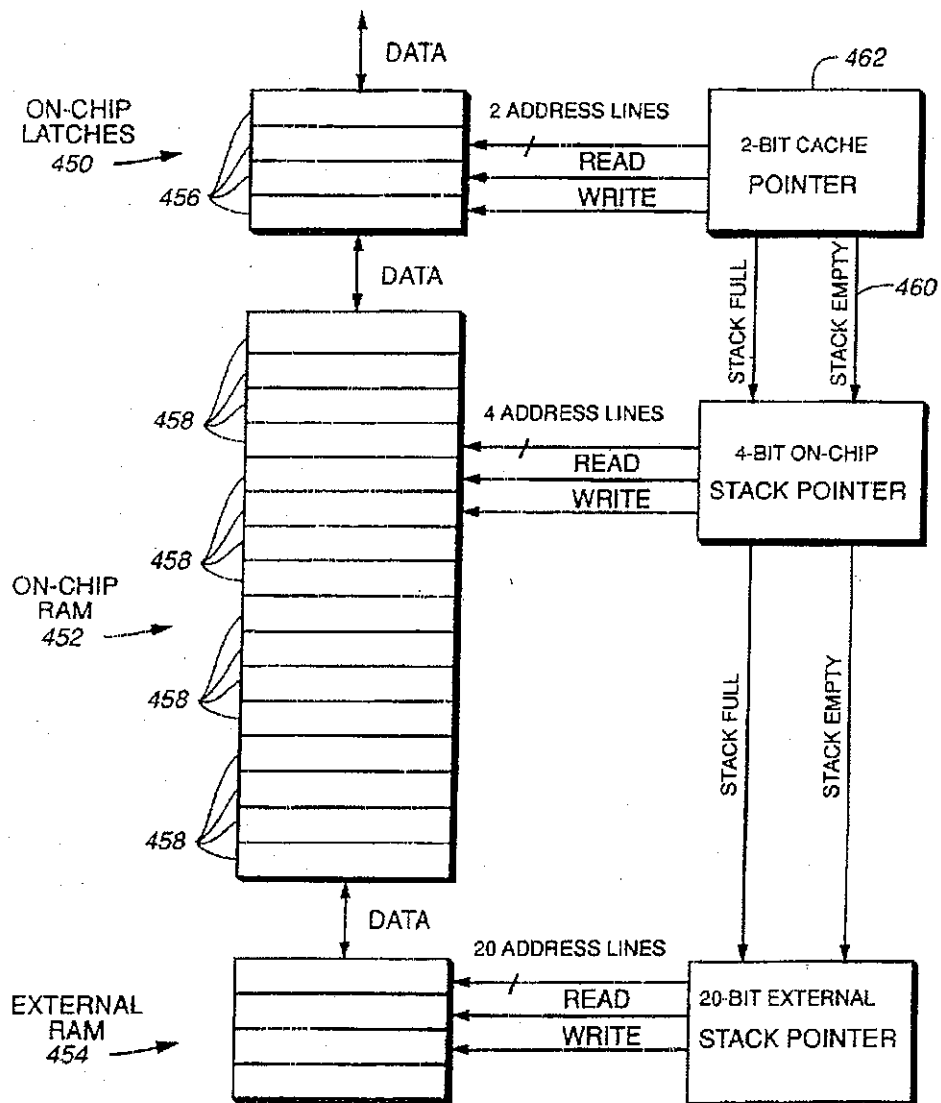


FIG. 21

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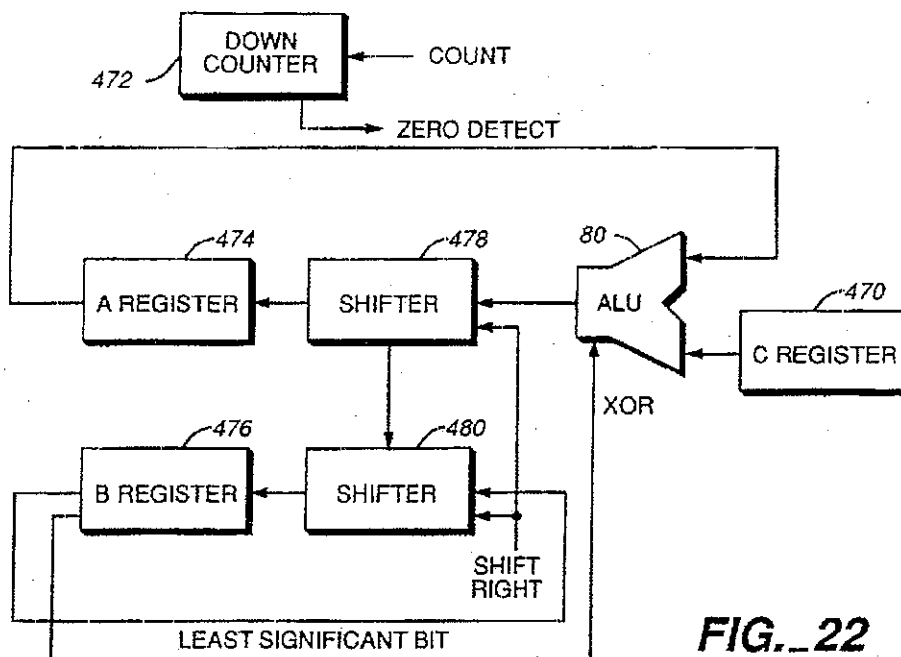


FIG. 22

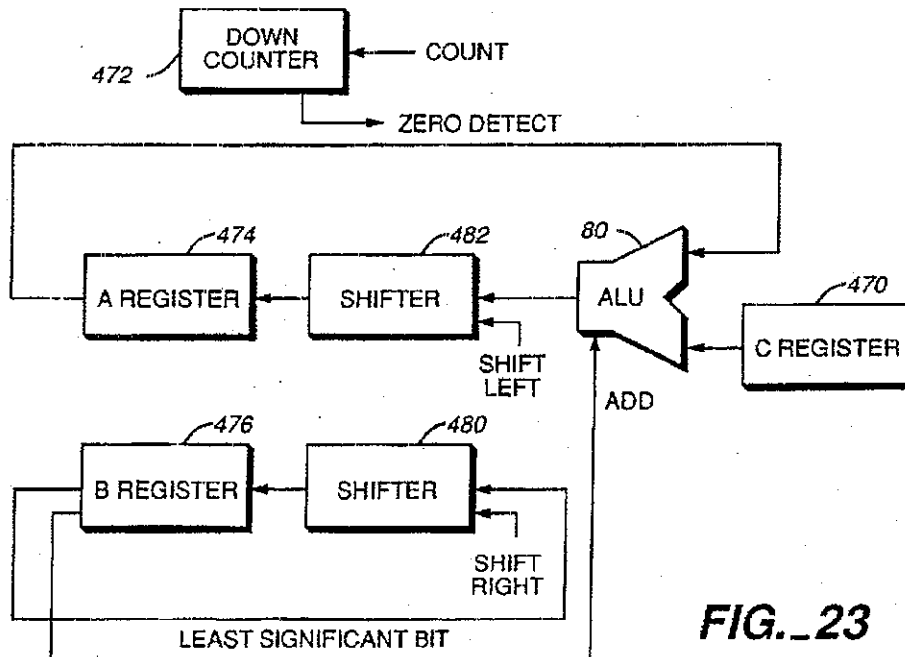


FIG. 23

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HIGH PERFORMANCE MICROPROCESSOR USING INSTRUCTIONS THAT OPERATE WITHIN INSTRUCTION GROUPS

This application is a division of U.S. application Ser. No. 07/389,334 filed Aug. 3, 1989, now U.S. Pat. No. 5,440,749.

BACKGROUND OF THE INVENTION

1 Field of the Invention

The present invention relates generally to a simplified reduced instruction set computer (RISC) microprocessor. More particularly, it relates to such a microprocessor which is capable of performance levels of, for example, 20 million instructions per second (MIPS) at a price of, for example, 20 dollars.

2 Description of the Prior Art

Since the invention of the microprocessor, improvements in its design have taken two different approaches. In the first approach, a brute force gain in performance has been achieved through the provision of greater numbers of faster transistors in the microprocessor integrated circuit and an instruction set of increased complexity. This approach is exemplified by the Motorola 68000 and Intel 80X86 microprocessor families. The trend in this approach is to larger die sizes and packages, with hundreds of pinouts.

More recently, it has been perceived that performance gains can be achieved through comparative simplicity, both in the microprocessor integrated circuit itself and in its instruction set. This second approach provides RISC microprocessors, and is exemplified by the Sun SPARC and the Intel 8960 microprocessors. However, even with this approach as conventionally practiced, the packages for the microprocessor are large, in order to accommodate the large number of pinouts that continue to be employed. A need therefore remains for further simplification of high performance microprocessors.

With conventional high performance microprocessors fast static memories are required for direct connection to the microprocessors in order to allow memory accesses that are fast enough to keep up with the microprocessors. Slower dynamic random access memories (DRAMs) are used with such microprocessors only in a hierarchical memory arrangement with the static memories acting as a buffer between the microprocessors and the DRAMs. The necessity to use static memories increases cost of the resulting systems.

Conventional microprocessors provide direct memory accesses (DMA) for system peripheral units through DMA controllers, which may be located on the microprocessor integrated circuit or provided separately. Such DMA controllers can provide routine handling of DMA requests and responses, but some processing by the main central processing unit (CPU) of the microprocessor is required.

SUMMARY OF THE INVENTION

Accordingly, it is an object of this invention to provide a microprocessor with a reduced pin count and cost compared to conventional microprocessors.

It is another object of the invention to provide a high performance microprocessor that can be directly connected to DRAMs without sacrificing microprocessor speed.

It is a further object of the invention to provide a high performance microprocessor in which DMA does not require use of the main CPU during DMA requests and

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responses and which provides very rapid DMA response with predictable response times.

The attainment of these and related objects may be achieved through use of the novel high performance low cost microprocessor herein disclosed. In accordance with one aspect of the invention, a microprocessor system in accordance with this invention has a central processing unit, a memory and a bus connecting the central processing unit to the memory. Instruction fetching means are connected to the bus to fetch instruction groups via the bus from the memory. Each of the instruction groups include at least one instruction that accesses operands or instructions or both. The operands and instructions are located relative to the instruction groups. An instruction register receives a first of the instruction groups from the instruction fetching means. The first of the instruction groups include one or more sequential instructions. Instruction supplying means supplies, in succession from the instruction register, the one or more sequential instructions of the first of the instruction groups to the central processing unit. An instruction decoding means configures the instruction supplying means to select from the instruction register an operand associated with one of the instructions from the first of the instruction groups.

In accordance with another aspect of the invention, the microprocessor has a central processing unit and an instruction register operatively coupled to the central processing unit. An instruction fetching means provides instruction groups to the instruction register wherein certain of the instruction groups include one or more operands or sequential instructions or both. The one or more sequential instructions including at least one instruction that accesses operands or instructions or both being located relative to the instruction groups. An instruction supplying means successively couples the one or more sequential instructions of the certain of the instruction groups to the central processing unit. An instruction decoding means configures the instruction supplying means to select operands from the instruction register associated with particular ones of the sequential instructions.

In another aspect of the invention, the microprocessor system includes a central processing unit, memory, and an instruction register. A method provides instructions from the instruction register to the central processing unit and comprises the steps of:

providing instruction groups to the instruction register from the memory wherein certain of the instruction groups include one or more operands or sequential instructions or both;

supplying, in succession from the instruction register, the one or more sequential instructions of the certain of the instruction groups to the central processing unit; and selecting an operand from the one of the instruction groups for use by the central processing unit.

The attainment of the foregoing and related objects, advantages and features of the invention should be more readily apparent to those skilled in the art, after review of the following more detailed description of the invention taken together with the drawings in which:

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is an external, plan view of an integrated circuit package incorporating a microprocessor in accordance with the invention.

FIG. 2 is a block diagram of a microprocessor in accordance with the invention.

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FIG. 3 is a block diagram of a portion of a data processing system incorporating the microprocessor of FIGS. 1 and 2.

FIG. 4 is a more detailed block diagram of a portion of the microprocessor shown in FIG. 2.

FIG. 5 is a more detailed block diagram of another portion of the microprocessor shown in FIG. 2.

FIG. 6 is a block diagram of another portion of the data processing system shown in part in FIG. 3 and incorporating the microprocessor of FIGS. 1-2 and 4-5.

FIGS. 7 and 8 are layout diagrams for the data processing system shown in part in FIGS. 3 and 6.

FIG. 9 is a layout diagram of a second embodiment of a microprocessor in accordance with the invention in a data processing system on a single integrated circuit.

FIG. 10 is a more detailed block diagram of a portion of the data processing system of FIGS. 7 and 8.

FIG. 11 is a timing diagram useful for understanding operation of the system portion shown in FIG. 12.

FIG. 12 is another more detailed block diagram of a further portion of the data processing system of FIGS. 7 and 8.

FIG. 13 is a more detailed block diagram of a portion of the microprocessor shown in FIG. 2.

FIG. 14 is a more detailed block and schematic diagram of a portion of the system shown in FIGS. 3 and 7-8.

FIG. 15 is a graph useful for understanding operation of the system portion shown in FIG. 14.

FIG. 16 is a more detailed block diagram showing part of the system portion shown in FIG. 4.

FIG. 17 is a more detailed block diagram of a portion of the microprocessor shown in FIG. 2.

FIG. 18 is a more detailed block diagram of part of the microprocessor portion shown in FIG. 17.

FIG. 19 is a set of waveform diagrams useful for understanding operation of the part of the microprocessor portion shown in FIG. 18.

FIG. 20 is a more detailed block diagram showing another part of the system portion shown in FIG. 4.

FIG. 21 is a more detailed block diagram showing another part of the system portion shown in FIG. 4.

FIGS. 22 and 23 are more detailed block diagrams showing another part of the system portion shown in FIG. 4.

DETAILED DESCRIPTION OF THE INVENTION

OVERVIEW

The microprocessor of this invention is desirably implemented as a 32-bit microprocessor optimized for:

HIGH EXECUTION SPEED, and

LOW SYSTEM COST.

In this embodiment, the microprocessor can be thought of as 20 MIPS for 20 dollars. Important distinguishing features of the microprocessor are:

Uses low-cost commodity DYNAMIC RAMS to run 20 MIPS

4 instruction fetch per memory cycle

On-chip fast page-mode memory management

Runs fast without external cache

Requires few interfacing chips

Crams 32-bit CPU in 44 pin SOJ package

The instruction set is organized so that most operations can be specified with 8-bit instructions. Two positive products of this philosophy are:

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Programs are smaller

Programs can execute much faster

The bottleneck in most computer systems is the memory bus. The bus is used to fetch instructions and fetch and store data. The ability to fetch four instructions in a single memory bus cycle significantly increases the bus availability to handle data.

Turning now to the drawings, more particularly to FIG. 1, there is shown a packaged 32-bit microprocessor 50 in a 44-pin plastic leadless chip carrier, shown approximately 100 times its actual size of about 0.8 inch on a side. The fact that the microprocessor 50 is provided as a 44-pin package represents a substantial departure from typical microprocessor packages, which usually have about 200 input/output (I/O) pins. The microprocessor 50 is rated at 20 million instructions per second (MIPS). Address and data lines 52, also labelled D0-D31, are shared for addresses and data without speed penalty as a result of the manner in which the microprocessor 50 operates, as will be explained below.

DYNAMIC RAM

In addition to the low cost 44-pin package, another unusual aspect of the high performance microprocessor 50 is that it operates directly with dynamic random access memories (DRAMs), as shown by row address strobe (RAS) and column address strobe (CAS) I/O pins 54. The other I/O pins for the microprocessor 50 include V_{DD} pins 56, V_{SS} pins 58, output enable pin 60, write pin 62, clock pin 64 and reset pin 66.

All high speed computers require high speed and expensive memory to keep up. The highest speed static RAM memories cost as much as ten times as much as slower dynamic RAMs. This microprocessor has been optimized to use low-cost dynamic RAM in high-speed page-mode. Page-mode dynamic RAMs offer static RAM performance without the cost penalty. For example, low-cost 85 nsec. dynamic RAMs access at 25 nsec when operated in fast page-mode. Integrated fast page-mode control on the microprocessor chip simplifies system interfacing and results in a faster system.

Details of the microprocessor 50 are shown in FIG. 2. The microprocessor 50 includes a main central processing unit (CPU) 70 and a separate direct memory access (DMA) CPU 72 in a single integrated circuit making up the microprocessor 50. The main CPU 70 has a first 16 deep push down stack 74, which has a top item register 76 and a next item register 78, respectively connected to provide inputs to an arithmetic logic unit (ALU) 80 by lines 82 and 84. An output of the ALU 80 is connected to the top item register 76 by line 86. The output of the top item register at 82 is also connected by line 88 to an internal data bus 90.

A loop counter 92 is connected to a decremented 94 by lines 96 and 98. The loop counter 92 is bidirectionally connected to the internal data bus 90 by line 100. Stack pointer 102, return stack pointer 104, mode register 106 and instruction register 108 are also connected to the internal data bus 90 by lines 110, 112, 114 and 116, respectively. The internal data bus 90 is connected to memory controller 118 and to gate 120. The gate 120 provides inputs on lines 122, 124, and 126 to X register 128, program counter 130 and Y register 132 of return push down stack 134. The X register 128, program counter 130 and Y register 132 provide outputs to internal address bus 136 on lines 138, 140 and 142. The internal address bus provides inputs to the memory controller 118 and to an incrementer 144. The incrementer 144 provides inputs to the X register, program counter and Y register via lines 146, 122, 124 and 126. The DMA CPU 72 provides inputs to the memory controller 118 on line 148.

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The memory controller 118 is connected to a RAM (not shown) by address/data bus 151 and control lines 153.

FIG. 2 shows that the microprocessor 50 has a simple architecture. Prior art RISC microprocessors are substantially more complex in design. For example, the SPARC RISC microprocessor has three times the gates of the microprocessor 50, and the Intel 8960 RISC microprocessor has 20 times the gates of the microprocessor 50. The speed of this microprocessor is in substantial part due to this simplicity. The architecture incorporates push down stacks and register write to achieve this simplicity.

The microprocessor 50 incorporates an I/O that has been tuned to make heavy use of resources provided on the integrated circuit chip. On chip latches allow use of the same I/O circuits to handle three different things: column addressing, row addressing and data, with a slight to non-existent speed penalty. This triple bus multiplexing results in fewer buffers to expand, fewer interconnection lines, fewer I/O pins and fewer internal buffers.

The provision of on-chip DRAM control gives a performance equal to that obtained with the use of static RAMs. As a result, memory is provided at 1/4 the system cost of static RAM used in most RISC systems.

The microprocessor 50 fetches 4 instructions per memory cycle; the instructions are in an 8-bit format, and this is a 32-bit microprocessor. System speed is therefore 4 times the memory bus bandwidth. This ability enables the microprocessor to break the Von Neumann bottleneck of the speed of getting the next instruction. This mode of operation is possible because of the use of a push down stack and register array. The push down stack allows the use of implied addresses, rather than the prior art technique of explicit addresses for two sources and a destination.

Most instructions execute in 20 nanoseconds in the microprocessor 50. The microprocessor can therefore execute instructions at 50 peak MIPS without pipeline delays. This is a function of the small number of gates in the microprocessor 50 and the high degree of parallelism in the architecture of the microprocessor.

FIG. 3 shows how column and row addresses are multiplexed on lines D8-D14 of the microprocessor 50 for addressing DRAM 150 from I/O pins 52. The DRAM 150 is one of eight, but only one DRAM 150 has been shown for clarity. As shown, the lines D11-D18 are respectively connected to row address inputs A0-A8 of the DRAM 150. Additionally, lines D12-D15 are connected to the data inputs DQ1-DQ4 of the DRAM 150. The output enable, write and column address strobe pins 54 are respectively connected to the output enable, write and column address strobe inputs of the DRAM 150 by lines 152. The row address strobe pin 54 is connected through row address strobe decode logic 154 to the row address strobe input of the DRAM 150 by lines 156 and 158.

D0-D7 pins 52 (FIG. 1) are idle when the microprocessor 50 is outputting multiplexed row and column addresses on D11-D18 pins 52. The D0-D7 pins 52 can therefore simultaneously be used for I/O when right justified I/O is desired. Simultaneous addressing and I/O can therefore be carried out.

FIG. 4 shows how the microprocessor 50 is able to achieve performance equal to the use of static RAMs with DRAMs through multiple instruction fetch in a single clock cycle and instruction fetch-ahead. Instruction register 108 receives four 8-bit byte instruction words 1-4 on 32-bit internal data bus 90. The four instruction byte 1-4 locations of the instruction register 108 are connected to multiplexer 170 by busses 172, 174, 176 and 178, respectively. A

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microprogram counter 180 is connected to the multiplexer 170 by lines 182. The multiplexer 170 is connected to decoder 184 by bus 186. The decoder 184 provides internal signals to the rest of the microprocessor 50 on lines 188.

Most significant bits 190 of each instruction byte 1-4 location are connected to a 4-input decoder 192 by lines 194. The output of decoder 192 is connected to memory controller 118 by line 196. Program counter 130 is connected to memory controller 118 by internal address bus 136, and the instruction register 108 is connected to the memory controller 118 by the internal data bus 90. Address/data bus 198 and control bus 200 are connected to the DRAMs 150 (FIG. 3).

In operation, when the most significant bits 190 of remaining instructions 1-4 are "1" in a clock cycle of the microprocessor 50, there are no memory reference instructions in the queue. The output of decoder 192 on line 196 requests an instruction fetch ahead by memory controller 118 without interference with other accesses. While the current instructions in instruction register 108 are executing, the memory controller 118 obtains the address of the next set of four instructions from program counter 130 and obtains that set of instructions. By the time the current set of instructions has completed execution, the next set of instructions is ready for loading into the instruction register.

Details of the DMA CPU 72 are provided in FIG. 5. Internal data bus 90 is connected to memory controller 118 and to DMA instruction register 210. The DMA instruction register 210 is connected to DMA program counter 212 by bus 214, to transfer size counter 216 by bus 218 and to timed transfer interval counter 220 by bus 222. The DMA instruction register 210 is also connected to DMA I/O and RAM address register 224 by line 226. The DMA I/O and RAM address register 224 is connected to the memory controller 118 by memory cycle request line 228 and bus 230. The DMA program counter 212 is connected to the internal address bus 136 by bus 232. The transfer size counter 216 is connected to a DMA instruction done decrementer 234 by lines 236 and 238. The decrementer 234 receives a control input on memory cycle acknowledge line 240. When transfer size counter 216 has completed its count, it provides a control signal to DMA program counter 212 on line 242. Timed transfer interval counter 220 is connected to decrementer 244 by lines 246 and 248. The decrementer 244 receives a control input from a microprocessor system clock on line 250.

The DMA CPU 72 controls itself and has the ability to fetch and execute instructions. It operates as a co-processor to the main CPU 70 (FIG. 2) for time specific processing.

FIG. 6 shows how the microprocessor 50 is connected to an electrically programmable read only memory (EPROM) 260 by reconfiguring the data lines 52 so that some of the data lines 52 are input lines and some of them are output lines. Data lines 52 D0-D7 provide data to and from corresponding data terminals 262 of the EPROM 260. Data lines 52 D9-D18 provide addresses to address terminals 264 of the EPROM 260. Data lines 52 D19-D31 provide inputs from the microprocessor 50 to memory and I/O decode logic 266. RAS 0/1 control line 268 provides a control signal for determining whether the memory and I/O decode logic provides a DRAM RAS output on line 270 or a column enable output for the EPROM 260 on line 272. Column address strobe terminal 60 of the microprocessor 50 provides an output enable signal on line 274 to the corresponding terminal 276 of the EPROM 260.

FIGS. 7 and 8 show the front and back of a one card data processing system 280 incorporating the microprocessor 50, MSM514258-10 type DRAMs 150 totalling 2 megabytes a

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Motorola 50 MegaHertz crystal oscillator clock 282. I/O circuits 284 and a 27256 type EPROM 260. The I/O circuits 284 include a 74HC04 type high speed hex inverter circuit 286, an IDT39C828 type 10-bit inverting buffer circuit 288, an IDT39C822 type 10-bit inverting register circuit 290, and two IDT39C823 type 9-bit non-inverting register circuits 292. The card 280 is completed with a MAX12V type DC-DC converter circuit 294, 34-pin dual AMP type headers 296, a coaxial female power connector 298, and a 3-pin AMP right angle header 300. The card 280 is a low cost, imbeddable product that can be incorporated in larger systems or used as an internal development tool.

The microprocessor 50 is a very high performance (50 MHz) RISC influenced 32-bit CPU designed to work closely with dynamic RAM. Clock for clock, the microprocessor 50 approaches the theoretical performance limits possible with a single CPU configuration. Eventually, the microprocessor 50 and any other processor is limited by the bus bandwidth and the number of bus paths. The critical conduit is between the CPU and memory.

One solution to the bus bandwidth/bus path problem is to integrate a CPU directly onto the memory chips, giving every memory a direct bus to the CPU. FIG. 9 shows another microprocessor 310 that is provided integrally with 1 megabit of DRAM 311 in a single integrated circuit 312. Until the present invention, this solution has not been practical, because most high performance CPUs require from 500,000 to 1,000,000 transistors and enormous die sizes just by themselves. The microprocessor 310 is equivalent to the microprocessor 50 in FIGS. 1-8. The microprocessors 50 and 310 are the most transistor efficient high performance CPUs in existence, requiring fewer than 50,000 transistors for dual processors 70 and 72 (FIG. 2) or 314 and 316 (less memory). The very high speed of the microprocessors 50 and 310 is to a certain extent a function of the small number of active devices. In essence, the less silicon gets in the way, the faster the electrons can get where they are going.

The microprocessor 310 is therefore the only CPU suitable for integration on the memory chip die 312. Some simple modifications to the basic microprocessor 50 to take advantage of the proximity to the DRAM array 311 can also increase the microprocessor 50 clock speed by 50 percent, and probably more.

The microprocessor 310 core on board the DRAM die 312 provides most of the speed and functionality required for a large group of applications from automotive to peripheral control. However, the integrated CPU 310/DRAM 311 concept has the potential to redefine significantly the way multiprocessor solutions can solve a spectrum of very compute intensive problems. The CPU 310/DRAM 311 combination eliminates the Von Neumann bottleneck by distributing it across numerous CPU/DRAM chips 312. The microprocessor 310 is a particularly good core for multiprocessing, since it was designed with the SDI targeting array in mind, and provisions were made for efficient interprocessor communications.

Traditional multiprocessor implementations have been very expensive in addition to being unable to exploit fully the available CPU horsepower. Multiprocessor systems have typically been built up from numerous board level or box level computers. The result is usually an immense amount of hardware with corresponding wiring, power consumption and communications problems. By the time the systems are interconnected, as much as 50 percent of the bus speed has been utilized just getting through the interfaces.

In addition, multiprocessor system software has been scarce. A multiprocessor system can easily be crippled by an

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inadequate load-sharing algorithm in the system software which allows one CPU to do a great deal of work and the others to be idle. Great strides have been made recently in systems software, and even UNIX V.4 may be enhanced to support multiprocessing. Several commercial products from such manufacturers as DUAL Systems and UNISOFT do a credible job on 68030 type microprocessor systems now.

The microprocessor 310 architecture eliminates most of the interface friction, since up to 64 CPU 310/RAM 311 processors should be able to intercommunicate without buffers or latches. Each chip 312 has about 40 MIPS raw speed because placing the DRAM 311 next to the CPU 310 allows the microprocessor 310 instruction cycle to be cut in half, compared to the microprocessor 50. A 64 chip array of these chips 312 is more powerful than any other existing computer. Such an array fits on a 3x5 card, cost less than a FAX machine, and draw about the same power as a small television.

Dramatic changes in price/performance always reshape existing applications and almost always create new ones. The introduction of microprocessors in the mid 1970s created video games, personal computers, automotive computers, electronically controlled appliances, and low cost computer peripherals.

The integrated circuit 312 will find applications in all of the above areas, plus create some new ones. A common generic parallel processing algorithm handles convolution/Fast Fourier Transform (FFT)/pattern recognition. Interesting product possibilities using the integrated circuit 312 include high speed reading machines, real-time speech recognition, spoken language translation, real-time robot vision, a product to identify people by their faces, and an automotive or aviation collision avoidance system.

A real time processor for enhancing high density television (HDTV) images, or compressing the HDTV information into a smaller bandwidth, would be very feasible. The load sharing in HDTV could be very straightforward. Splitting up the task according to color and frame would require 6, 9 or 12 processors. Practical implementation might require 4 meg RAMs integrated with the microprocessor 310.

The microprocessor 310 has the following specifications:

CONTROL LINES
4—POWER/GROUND
1—CLOCK
32—DATA I/O
4—SYSTEM CONTROL
EXTERNAL MEMORY FETCH
EXTERNAL MEMORY FETCH AUTOINCREMENT X
EXTERNAL MEMORY FETCH AUTOINCREMENT Y
EXTERNAL MEMORY WRITE
EXTERNAL MEMORY WRITE AUTOINCREMENT X
EXTERNAL MEMORY WRITE AUTOINCREMENT Y
EXTERNAL PROM FETCH
LOAD ALL X REGISTERS
LOAD ALL Y REGISTERS
LOAD ALL PC REGISTERS
EXCHANGE X AND Y
INSTRUCTION FETCH
ADD TO PC
ADD TO X
WRITE MAPPING REGISTER
READ MAPPING REGISTER
REGISTER CONFIGURATION

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MICROPROCESSOR 310 CPU 316 CORE
 COLUMN LATCH1 (1024 BITS) 32x32 MUX
 STACK POINTER (16 BITS)
 COLUMN LATCH2 (1024 BITS) 32x32 MUX
 RSTACK POINTER (16 BITS)
 PROGRAM COUNTER 32 BITS
 XO REGISTER 32 BITS (ACTIVATED ONLY FOR
 ON-CHIP ACCESSES)
 YO REGISTER 32 BITS (ACTIVATED ONLY FOR
 ON-CHIP ACCESSES)
 LOOP COUNTER 32 BITS
 DMA CPU 314 CORE
 DMA PROGRAM COUNTER 24 BITS
 INSTRUCTION REGISTER 32 BITS
 I/O & RAM ADDRESS REGISTER 32 BITS
 TRANSFER SIZE COUNTER 12 BITS
 INTERVAL COUNTER 12 BITS

To offer memory expansion for the basic chip 312, an intelligent DRAM can be produced. This chip will be optimized for high speed operation with the integrated circuit 312 by having three on-chip address registers: Program Counter, X Register and Y register. As a result to access the intelligent DRAM, no address is required, and a total access cycle could be as short as 10 nsec. Each expansion DRAM would maintain its own copy of the three registers and would be identified by a code specifying its memory address. Incrementing and adding to the three registers will actually take place on the memory chips. A maximum of 64 intelligent DRAM peripherals would allow a large system to be created without sacrificing speed by introducing multiplexers or buffers.

There are certain differences between the microprocessor 310 and the microprocessor 50 that arise from providing the microprocessor 310 on the same die 312 with the DRAM 311. Integrating the DRAM 311 allows architectural changes in the microprocessor 310 logic to take advantage of existing on-chip DRAM 311 circuitry. Row and column design is inherent in memory architecture. The DRAMs 311 access random bits in a memory array by first selecting a row of 1024 bits, storing them into a column latch, and then selecting one of the bits as the data to be read or written.

The time required to access the data is split between the row access and the column access. Selecting data already stored in a column latch is faster than selecting a random bit by at least a factor of six. The microprocessor 310 takes advantage of this high speed by creating a number of column latches and using them as caches and shift registers. Selecting a new row of information may be thought of as performing a 1024-bit read or write with the resulting immense bus bandwidth.

1. The microprocessor 50 treats its 32-bit instruction register 108 (see FIGS. 2 and 4) as a cache for four 8-bit instructions. Since the DRAM 311 maintains a 1024-bit latch for the column bits, the microprocessor 310 treats the column latch as a cache for 128 8-bit instructions. Therefore, the next instruction will almost always be already present in the cache. Long loops within the cache are also possible and more useful than the 4 instruction loops in the microprocessor 50.

2. The microprocessor 50 uses two 16x32-bit deep register arrays 74 and 134 (FIG. 2) for the parameter stack and the return stack. The microprocessor 310 creates two other 1024-bit column latches to provide the equivalent of two 32x32-bit arrays, which can be accessed twice as fast as a register array.

3. The microprocessor 50 has a DMA capability which can be used for I/O to a video shift register. The micropro-

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cessor 310 uses yet another 1024-bit column latch as a long video shift register to drive a CRT display directly. For color displays, three on-chip shift registers could also be used. These shift registers can transfer pixels at a maximum of 100 MHz.

4. The microprocessor 50 accesses memory via an external 32-bit bus. Most of the memory 311 for the microprocessor 310 is on the same die 312. External access to more memory is made using an 8-bit bus. The result is a smaller die, smaller package and lower power consumption than the microprocessor 50.

5. The microprocessor 50 consumes about a third of its operating power charging and discharging the I/O pins and associated capacitances. The DRAMs 150 (FIG. 8) connected to the microprocessor 50 dissipate most of their power in the I/O drivers. A microprocessor 310 system will consume about one-tenth the power of a microprocessor 50 system, since having the DRAM 311 next to the processor 310 eliminates most of the external capacitances to be charged and discharged.

6. Multiprocessing means splitting a computing task between numerous processors in order to speed up the solution. The popularity of multiprocessing is limited by the expense of current individual processors as well as the limited interprocessor communications ability. The microprocessor 310 is an excellent multiprocessor candidate, since the chip 312 is a monolithic computer complete with memory, rendering it low-cost and physically compact.

The shift registers implemented with the microprocessor 310 to perform video output can also be configured as interprocessor communication links. The INMOS transputer attempted a similar strategy, but at much lower speed and without the performance benefits inherent in the microprocessor 310 column latch architecture. Serial I/O is a prerequisite for many multiprocessor topologies because of the many neighbor processors which communicate. A cube has 6 neighbors. Each neighbor communicates using these lines:

DATA IN
 CLOCK IN
 READY FOR DATA
 DATA OUT
 DATA READY?
 CLOCK OUT

A special start up sequence is used to initialize the on-chip DRAM 311 in each of the processors.

The microprocessor 310 column latch architecture allows neighbor processors to deliver information directly to internal registers or even instruction caches of other chips 312. This technique is not used with existing processors, because it only improves performance in a tightly coupled DRAM system.

7. The microprocessor 50 architecture offers two types of looping structures: LOOP-IF-DONE and MICRO-LOOP. The former takes an 8-bit to 24-bit operand to describe the entry point to the loop address. The latter performs a loop entirely within the 4 instruction queue and the loop entry point is implied as the first instruction in the queue. Loops entirely within the queue run without external instruction fetches and execute up to three times as fast as the long loop construct. The microprocessor 310 retains both constructs with a few differences. The microprocessor 310 microloop functions in the same fashion as the microprocessor 50 operation, except the queue is 1024-bits or 128 8-bit instructions long. The microprocessor 310 microloop can therefore contain jumps, branches, calls and immediate operations not possible in the 4 8-bit instruction microprocessor 50 queue.

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Microloops in the microprocessor 50 can only perform simple block move and compare functions. The larger microprocessor 310 queue allows entire digital signal processing or floating point algorithms to loop at high speed in the queue.

The microprocessor 50 offers four instructions to redirect execution:

CALL
BRANCH
BRANCH-IF-ZERO
LOOP-IF-NOT-DONE

These instructions take a variable length address operand 8, 16 or 24 bits long. The microprocessor 50 next address logic treats the three operands similarly by adding or subtracting them to the current program counter. For the microprocessor 310, the 16 and 24-bit operands function in the same manner as the 16 and 24-bit operands in the microprocessor 50. The 8-bit class operands are reserved to operate entirely within the instruction queue. Next address decisions can therefore be made quickly, because only 10 bits of addresses are affected, rather than 32. There is no carry or borrow generated past the 10 bits.

8 The microprocessor 310 CPU 316 resides on an already crowded DRAM die 312. To keep chip size as small as possible, the DMA processor 72 of the microprocessor 50 has been replaced with a more traditional DMA controller 314. DMA is used with the microprocessor 310 to perform the following functions:

Video output to a CRT
Multiprocessor serial communications
8-bit parallel I/O

The DMA controller 314 can maintain both serial and parallel transfers simultaneously. The following DMA sources and destinations are supported by the microprocessor 310:

DESCRIPTION	I/O	LINES
1 Video shift register	OUTPUT	1 to 3
2 Multiprocessor serial	BOTH	6 lines/channel
3 8-bit parallel	BOTH	8 data, 4 control

The three sources use separate 1024-bit buffers and separate I/O pins. Therefore, all three may be active simultaneously without interference.

The microprocessor 310 can be implemented with either a single multiprocessor serial buffer or separate receive and sending buffers for each channel, allowing simultaneous bidirectional communications with six neighbors simultaneously.

FIGS 10 and 11 provide details of the PROM DMA used in the microprocessor 50. The microprocessor 50 executes faster than all but the fastest PROMs. PROMs are used in a microprocessor 50 system to store program segments and perhaps entire programs. The microprocessor 50 provides a feature on power-up to allow programs to be loaded from low-cost, slow speed PROMs into high speed DRAM for execution. The logic which performs this function is part of the DMA memory controller 118. The operation is similar to DMA, but not identical, since four 8-bit bytes must be assembled on the microprocessor 50 chip, then written to the DRAM 150.

The microprocessor 50 directly interfaces to DRAM 150 over a triple multiplexed data and address bus 350, which carries RAS addresses, CAS addresses and data. The EPROM 260 on the other hand, is read with non-

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multiplexed busses. The microprocessor 50 therefore has a special mode which unmultiplexes the data and address lines to read 8 bits of EPROM data. Four 8-bit bytes are read in this fashion. The multiplexed bus 350 is turned back on, and the data is written to the DRAM 150.

When the microprocessor 50 detects a RSEI condition, the processor stops the main CPU 70 and forces a mode 0 (PROM LOAD) instruction into the DMA CPU 72 instruction register. The DMA instruction directs the memory controller to read the EPROM 260 data at 8 times the normal access time for memory. Assuming a 50 MHz microprocessor 50, this means an access time of 320 nsec. The instruction also indicates:

The selection address of the EPROM 260 to be loaded.
The number of 32-bit words to transfer
The DRAM 150 address to transfer into.

The sequence of activities to transfer one 32-bit word from EPROM 260 to DRAM 150 are:

- 1 RAS goes low at 352, latching the EPROM 260 select information from the high order address bits. The EPROM 260 is selected.
- 2 Twelve address bits (consisting of what is normally DRAM CAS addresses plus two byte select bits) are placed on the bus 350 going to the EPROM 260 address pins. These signals will remain on the lines until the data from the EPROM 260 has been read into the microprocessor 50. For the first byte, the byte select bits will be binary 00.
- 3 CAS goes low at 354, enabling the EPROM 260 data onto the lower 8 bits of the external address/data bus 350. NOTE: It is important to recognize that, during this part of the cycle, the lower 8 bits of the external data/address bus are functioning as inputs but the rest of the bus is still acting as outputs.
- 4 The microprocessor 50 latches these eight least significant bits internally and shifts them 8 bits left to shift them to the next significant byte position.
- 5 Steps 2, 3 and 4 are repeated with byte address 01.
- 6 Steps 2, 3 and 4 are repeated with byte address 10.
- 7 Steps 2, 3 and 4 are repeated with byte address 11.
- 8 CAS goes high at 356, taking the EPROM 260 off the data bus.
- 9 RAS goes high at 358 indicating the end of the EPROM 260 access.
- 10 RAS goes low at 360, latching the DRAM select information from the high order address bits. At the same time, the RAS address bits are latched into the DRAM 150. The DRAM 150 is selected.
- 11 CAS goes low at 362 latching the DRAM 150 CAS addresses.
- 12 The microprocessor 50 places the previously latched EPROM 260 32-bit data onto the external address/data bus 350. W goes low at 364 writing the 32 bits into the DRAM 150.
- 13 W goes high at 366. CAS goes high at 368. The process continues with the next word.

FIG. 12 shows details of the microprocessor 50 memory controller 118. In operation, bus requests stay present until they are serviced. CPU 70 requests are prioritized at 370 in the order of: 1. Parameter Stack; 2. Return Stack; 3. Data Fetch; 4. Instruction Fetch. The resulting CPU request signal and a DMA request signal are supplied as bus requests to bus control 372, which provides a bus grant signal at 374. Internal address bus 136 and a DMA counter 376 provide inputs to a multiplexer 378. Either a row address or a column address are provided as an output to multiplexed address bus 380 as an output from the multiplexer 378. The multiplexed

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address bus 380 and the internal data bus 90 provide address and data inputs respectively, to multiplexer 382. Shift register 384 supplies row address strobe (RAS) 1 and 2 control signals to multiplexer 386 and column address strobe (CAS) 1 and 2 control signals to multiplexer 388 on lines 390 and 392. The shift register 384 also supplies output enable (OE) and write (W) signals on lines 394 and 396 and a control signal on line 398 to multiplexer 382. The shift register 384 receives a RUN signal on line 400 to generate a memory cycle and supplies a MEMORY READY signal on line 402 when an access is complete.

STACK/REGISTER ARCHITECTURE

Most microprocessors use on-chip registers for temporary storage of variables. The on-chip registers access data faster than off-chip RAM. A few microprocessors use an on-chip push down stack for temporary storage.

A stack has the advantage of faster operation compared to on-chip registers by avoiding the necessity to select source and destination registers. (A math or logic operation always uses the top two stack items as source and the top of stack as destination.) The stack's disadvantage is that it makes some operations clumsy. Some compiler activities in particular require on-chip registers for efficiency.

As shown in FIG. 13, the microprocessor 50 provides both on-chip registers 134 and a stack 74 and reaps the benefits of both.

BENEFITS:

- 1 Stack math and logic is twice as fast as those available on an equivalent register only machine. Most programmers and optimizing compilers can take advantage of this feature.
- 2 Sixteen registers are available for on-chip storage of local variables which can transfer to the stack for computation. The accessing of variables is three to four times as fast as available on a strictly stack machine.

The combined stack 74/register 134 architecture has not been used previously due to inadequate understanding by computer designers of optimizing compilers and the mix of transfer versus math/logic instructions.

ADAPTIVE MEMORY CONTROLLER

A microprocessor must be designed to work with small or large memory configurations. As more memory loads are added to the data, address, and control lines, the switching speed of the signals slows down. The microprocessor 50 multiplexes the address/data bus three ways, so timing between the phases is critical. A traditional approach to the problem allocates a wide margin of time between bus phases so that systems will work with small or large numbers of memory chips connected. A speed compromise of as much as 50% is required.

As shown in FIG. 14, the microprocessor 50 uses a feedback technique to allow the processor to adjust memory bus timing to be fast with small loads and slower with large ones. The OUTPUT ENABLE (OE) line 152 from the microprocessor 50 is connected to all memories 150 on the circuit board. The loading on the output enable line 152 to the microprocessor 50 is directly related to the number of memories 150 connected. By monitoring how rapidly OE 152 goes high after a read, the microprocessor 50 is able to determine when the data hold time has been satisfied and place the next address on the bus.

The level of the OE line 152 is monitored by CMOS input buffer 410 which generates an internal READY signal on line 412 to the microprocessor's memory controller. Curves 414 and 416 of the FIG. 15 graph show the difference in rise time likely to be encountered from a lightly to heavily loaded memory system. When the OE line 152 has reached

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a predetermined level to generate the READY signal driver 418 generates an OUTPUT ENABLE signal on OE line 152.

SKIP WITHIN THE INSTRUCTION CACHE

The microprocessor 50 fetches four 8-bit instructions each memory cycle and stores them in a 32-bit instruction register 108, as shown in FIG. 16. A class of "test and skip" instructions can very rapidly execute a very fast jump operation within the four instruction cache.

SKIP CONDITIONS:

- Always
- ACC non-zero
- ACC negative
- Carry flag equal logic one
- Never
- ACC equal zero
- ACC positive
- Carry flag equal logic zero

The SKIP instruction can be located in any of the four byte positions 420 in the 32-bit instruction register 108. If the test is successful, SKIP will jump over the remaining one, two, or three 8-bit instructions in the instruction register 108 and cause the next four-instruction group to be loaded into the register 108. As shown the SKIP operation is implemented by resetting the 2-bit microinstruction counter 180 to zero on line 422 and simultaneously latching the next instruction group into the register 108. Any instructions following the SKIP in the instruction register are overwritten by the new instructions and not executed.

The advantage of SKIP is that optimizing compilers and smart programmers can often use it in place of the longer conditional JUMP instruction. SKIP also makes possible microloops which exit when the loop counts down or when the SKIP jumps to the next instruction group. The result is very fast code.

Other machines (such as the PDP-8 and Data General NOVA) provide the ability to skip a single instruction. The microprocessor 50 provides the ability to skip up to three instructions.

MICROLOOP IN THE INSTRUCTION CACHE

The microprocessor 50 provides the MICROLOOP instruction to execute repetitively from one to three instructions residing in the instruction register 108. The microloop instruction works in conjunction with the LOOP COUNTER 92 (FIG. 2) connected to the internal data bus 90. To execute a microloop, the program stores a count in LOOP COUNTER 92. MICROLOOP may be placed in the first, second, third, or last byte 420 of the instruction register 108. If placed in the first position, execution will just create a delay equal to the number stored in LOOP COUNTER 92 times the machine cycle. If placed in the second, third, or last byte 420, when the microloop instruction is executed it will test the LOOP COUNT for zero. If zero, execution will continue with the next instruction. If not zero, the LOOP COUNTER 92 is decremented and the 2-bit microinstruction counter is cleared, causing the preceding instructions in the instruction register to be executed again.

Microloop is useful for block move and search operations. By executing a block move completely out of the instruction register 108, the speed of the move is doubled, since all memory cycles are used by the move rather than being shared with instruction fetching. Such a hardware implementation of microloops is much faster than conventional software implementation of a comparable function.

OPTIMAL CPU CLOCK SCHEME

The designer of a high speed microprocessor must produce a product which operate over wide temperature ranges.

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wide voltage swings, and wide variations in semiconductor processing. Temperature, voltage, and process all affect transistor propagation delays. Traditional CPU designs are done so that with the worse case of the three parameters, the circuit will function at the rated clock speed. The result are designs that must be clocked a factor of two slower than their maximum theoretical performance so they will operate properly in worse case conditions.

The microprocessor 50 uses the technique shown in FIGS 17-19 to generate the system clock and its required phases. Clock circuit 430 is the familiar "ring oscillator" used to test process performance. The clock is fabricated on the same silicon chip as the rest of the microprocessor 50.

The ring oscillator frequency is determined by the parameters of temperature, voltage, and process. At room temperature, the frequency will be in the neighborhood of 100 MHz. At 70 degrees Centigrade, the speed will be 50 MHz. The ring oscillator 430 is useful as a system clock, with its stages 431 producing phase 0-phase 3 outputs 433 shown in FIG 19, because its performance tracks the parameters which similarly affect all other transistors on the same silicon die. By deriving system timing from the ring oscillator 430, CPU 70 will always execute at the maximum frequency possible, but never too fast. For example if the processing of a particular die is not good resulting in slow transistors, the latches and gates on the microprocessor 50 will operate slower than normal. Since the microprocessor 50 ring oscillator clock 430 is made from the same transistors on the same die as the latches and gates, it too will operate slower (oscillating at a lower frequency), providing compensation which allows the rest of the chip's logic to operate properly.

ASYNCHRONOUS/SYNCHRONOUS CPU

Most microprocessors derive all system timing from a single clock. The disadvantage is that different parts of the system can slow all operations. The microprocessor 50 provides a dual-clock scheme as shown in FIG. 17, with the CPU 70 operating asynchronously to I/O interface 432 forming part of memory controller 118 (FIG. 2) and the I/O interface 432 operating synchronously with the external world of memory and I/O devices. The CPU 70 executes at the fastest speed possible using the adaptive ring counter clock 430. Speed may vary by a factor of four depending upon temperature, voltage, and process. The external world must be synchronized to the microprocessor 50 for operations such as video display updating and disc drive reading and writing. This synchronization is performed by the I/O interface 432, speed of which is controlled by a conventional crystal clock 434. The interface 432 processes requests for memory accesses from the microprocessor 50 and acknowledges the presence of I/O data. The microprocessor 50 fetches up to four instructions in a single memory cycle and can perform much useful work before requiring another memory access. By decoupling the variable speed of the CPU 70 from the fixed speed of the I/O interface 432, optimum performance can be achieved by each. Recoupling between the CPU 70 and the interface 432 is accomplished with handshake signals on lines 436 with data/addresses passing on bus 90, 136.

ASYNCHRONOUS/SYNCHRONOUS CPU IMBEDDED ON A DRAM CHIP

System performance is enhanced even more when the DRAM 311 and CPU 314 (FIG. 9) are located on the same die. The proximity of the transistors means that DRAM 311 and CPU 314 parameters will closely follow each other. At room temperature, not only would the CPU 314 execute at 100 MHz but the DRAM 311 would access fast enough to

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keep up. The synchronization performed by the I/O interface 432 would be for DMA and reading and writing I/O ports. In some systems (such as calculators) no I/O synchronization at all would be required, and the I/O clock would be tied to the ring counter clock.

VARIABLE WIDTH OPERANDS

Many microprocessors provide variable width operands. The microprocessor 50 handles operands of 8, 16, or 24 bits using the same op-code. FIG 20 shows the 32-bit instruction register 108 and the 2-bit microinstruction register 180 which selects the 8-bit instruction. Two classes of microprocessor 50 instructions can be greater than 8-bits. JUMP class and IMMEDIATE. A JUMP or IMMEDIATE op-code is 8-bits, but the operand can be 8, 16, or 24 bits long. This magic is possible because operands must be right justified in the instruction register. This means that the least significant bit of the operand is always located in the least significant bit of the instruction register. The microinstruction counter 180 selects which 8-bit instruction to execute. If a JUMP or IMMEDIATE instruction is decoded, the state of the 2-bit microinstruction counter selects the required 8, 16, or 24 bit operand onto the address or data bus. The unselected 8-bit bytes are loaded with zeros by operation of decoder 440 and gates 442. The advantage of this technique is the saving of a number of op-codes required to specify the different operand sizes in other microprocessors.

TRIPLE STACK CACHE

Computer performance is directly related to the system memory bandwidth. The faster the memories, the faster the computer. Fast memories are expensive so techniques have been developed to move a small amount of high-speed memory around to the memory addresses where it is needed. A large amount of slow memory is constantly updated by the fast memory, giving the appearance of a large fast memory array. A common implementation of the technique is known as a high-speed memory cache. The cache may be thought of as fast acting shock absorber smoothing out the bumps in memory access. When more memory is required than the shock can absorb, it bottoms out and slow speed memory is accessed. Most memory operations can be handled by the shock absorber itself.

The microprocessor 50 architecture has the ALU 80 (FIG 2) directly coupled to the top two stack locations 76 and 78. The access time of the stack 74 therefore directly affects the execution speed of the processor. The microprocessor 50 stack architecture is particularly suitable to a triple cache technique, shown in FIG. 21 which offers the appearance of a large stack memory operating at the speed of on-chip latches 450. Latches 450 are the fastest form of memory device built on the chip, delivering data in as little as 3 nsec. However latches 450 require large numbers of transistors to construct. On-chip RAM 452 requires fewer transistors than latches, but is slower by a factor of five (15 nsec access). Off-chip RAM 150 is the slowest storage of all. The microprocessor 50 organizes the stack memory hierarchy as three interconnected stacks 450, 452 and 454. The latch stack 450 is the fastest and most frequently used. The on-chip RAM stack 452 is next. The off-chip RAM stack 454 is slowest. The stack modulation determines the effective access time of the stack. If a group of stack operations never push or pull more than four consecutive items on the stack, operations will be entirely performed in the 3 nsec latch stack. When the four latches 456 are filled, the data in the bottom of the latch stack 450 is written to the top of the on-chip RAM stack 452. When the sixteen locations 458 in the on-chip RAM stack 452 are filled, the data in the bottom of the on-chip RAM stack 452 is written to the top of the off-chip

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RAM stack 454. When popping data off a full stack 450, four pops will be performed before stack empty line 460 from the latch stack pointer 462 transfers data from the on-chip RAM stack 452. By waiting for the latch stack 450 to empty before performing the slower on-chip RAM access, the high effective speed of the latches 456 are made available to the processor. The same approach is employed with the on-chip RAM stack 452 and the off-chip RAM stack 454.

POLYNOMIAL GENERATION INSTRUCTION

Polynomials are useful for error correction, encryption, data compression, and fractal generation. A polynomial is generated by a sequence of shift and exclusive OR operations. Special chips are provided for this purpose in the prior art.

The microprocessor 50 is able to generate polynomials at high speed without external hardware by slightly modifying how the ALU 80 works. As shown in FIG. 22, a polynomial is generated by loading the "order" (also known as the feedback terms) into C Register 470. The value thirty one (resulting in 32 iterations) is loaded into DOWN COUNTER 472. A register 474 is loaded with zero. B register 476 is loaded with the starting polynomial value. When the POLY instruction executes, C register 470 is exclusively ORED with A register 474 if the least significant bit of B register 476 is a one. Otherwise, the contents of the A register 474 passes through the ALU 80 unaltered. The combination of A and B is then shifted right (divided by 2) with shifters 478 and 480. The operation automatically repeats the specified number of iterations and the resulting polynomial is left in A register 474.

FAST MULTIPLY

Most microprocessors offer a 16x16 or 32x32 bit multiply instruction. Multiply when performed sequentially takes one shift/add per bit or 32 cycles for 32 bit data. The microprocessor 50 provides a high speed multiply which allows multiplication by small numbers using only a small number of cycles. FIG. 23 shows the logic used to implement the high speed algorithm. To perform a multiply, the size of the multiplier less one is placed in the DOWN COUNTER 472. For a four bit multiplier, the number three would be stored in the DOWN COUNTER 472. Zero is loaded into the A register 474. The multiplier is written bit reversed into the B Register 476. For example, a bit reversed five (binary 0101) would be written into B as 1010. The multiplicand is written into the C register 470. Executing the FAST MULT instruction will leave the result in the A Register 474, when the count has been completed. The fast multiply instruction is important because many applications scale one number by a much smaller number. The difference in speed between multiplying a 32x32 bit and a 32x4 bit is a factor of 8. If the least significant bit of the multiplier is a "ONE", the contents of the A register 474 and the C register 470 are added. If the least significant bit of the multiplier is a "ZERO", the contents of the A register are passed through the ALU 80 unaltered. The output of the ALU 80 is shifted left by shifter 482 in each iteration. The contents of the B register 476 are shifted right by the shifter 480 in each iteration.

INSTRUCTION EXECUTION PHILOSOPHY

The microprocessor 50 uses high speed D latches in most of the speed critical areas. Slower on-chip RAM is used as secondary storage.

The microprocessor 50 philosophy of instruction execution is to create a hierarchy of speed as follows:

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Logic and D latch transfers	1 cycle	20 nsec
Math	2 cycles	40 nsec
Fetch/store on-chip RAM	2 cycles	40 nsec
Fetch/store in current RAS page	4 cycles	80 nsec
Fetch/store with RAS cycle	11 cycles	220 nsec

With a 50 MHz clock, many operations can be performed in 20 nsec and almost everything else in 40 nsec.

To maximize speed, certain techniques in processor design have been used. They include:

- Eliminating arithmetic operations on addresses.
- Fetching up to four instructions per memory cycle.
- Pipelineless instruction decoding.
- Generating results before they are needed.
- Use of three level stack caching.

PIPELINE PHILOSOPHY

Computer instructions are usually broken down into sequential pieces, for example: fetch, decode, register read, execute, and store. Each piece will require a single machine cycle. In most Reduced Instruction Set Computer (RISC) chips, instruction require from three to six cycles.

RISC instructions are very parallel. For example, each of 70 different instructions in the SPARC (SUN Computer's RISC chip) has five cycles. Using a technique called "pipelining", the different phases of consecutive instructions can be overlapped.

To understand pipelining, think of building five residential homes. Each home will require in sequence, a foundation, framing, plumbing and wiring, roofing, and interior finish. Assume that each activity takes one week. To build one house will take five weeks.

But what if you want to build an entire subdivision? You have only one of each work crew, but when the foundation men finish on the first house, you immediately start them on the second one, and so on. At the end of five weeks, the first home is complete, but you also have five foundations. If you have kept the framing, plumbing, roofing, and interior guys all busy, from five weeks on, a new house will be completed each week.

This is the way a RISC chip like SPARC appears to execute an instruction in a single machine cycle. In reality, a RISC chip is executing one fifth of five instructions each machine cycle. And if five instructions stay in sequence, an instruction will be completed each machine cycle.

The problems with a pipeline are keeping the pipe full with instructions. Each time an out of sequence instruction such as a BRANCH or CALL occurs, the pipe must be refilled with the next sequence. The resulting dead time to refill the pipeline can become substantial when many IF/THEN/ELSE statements or subroutines are encountered.

THE PIPELINE APPROACH

The microprocessor 50 has no pipeline as such. The approach of this microprocessor to speed is to overlap instruction fetching with execution of the previously fetched instruction(s). Beyond that, over half the instructions (the most common ones) execute entirely in a single machine cycle of 20 nsec. This is possible because:

1. Instruction decoding resolves in 2.5 nsec.
2. Incremented/decremented and some math values are calculated before they are needed, requiring only a latching signal to execute.
3. Slower memory is hidden from high speed operations by high-speed D latches which access in 4 nsec.

The disadvantage for this microprocessor is a more complex chip design process. The advantage for the chip user is faster

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ultimate throughput since pipeline stalls cannot exist. Pipeline synchronization with availability flag bits and other such pipeline handling is not required by this microprocessor.

For example, in some RISC machines an instruction which tests a status flag may have to wait for up to four cycles for the flag set by the previous instruction to be available to be tested. Hardware and software debugging is also somewhat easier because the user doesn't have to visualize five instructions simultaneously in the pipe.

OVERLAPPING INSTRUCTION FETCH/EXECUTE

The slowest procedure the microprocessor 50 performs is to access memory. Memory is accessed when data is read or written. Memory is also read when instructions are fetched. The microprocessor 50 is able to hide fetch of the next instruction behind the execution of the previously fetched instruction(s). The microprocessor 50 fetches instructions in 4-byte instruction groups. An instruction group may contain from one to four instructions. The amount of time required to execute the instruction group ranges from 4 cycles for simple instructions to 64 cycles for a multiply.

When a new instruction group is fetched, the microprocessor instruction decoder looks at the most significant bit of all four of the bytes. The most significant bit of an instruction determines if a memory access is required. For example, CALL, FETCH, and STORE all require a memory access to execute. If all four bytes have nonzero most significant bits, the microprocessor initiates the memory fetch of the next sequential 4-byte instruction group. When the last instruction in the group finishes executing, the next 4-byte instruction group is ready and waiting on the data bus needing only to be latched into the instruction register. If the 4-byte instruction group required four or more cycles to execute and the next sequential access was a column address strobe (CAS) cycle, the instruction fetch was completely overlapped with execution.

INTERNAL ARCHITECTURE

The microprocessor 50 architecture consists of the following:

PARAMETER STACK <-> AIU*	Y REGISTER RETURN STACK
<-32 BITS-> 16 DEEP	<-32 BITS-> 16 DEEP
Used for math and logic	Used for subroutine and interrupt return addresses as well as local variables
Push down stack. Can overflow into off-chip RAM.	Push down stack. Can overflow into off-chip RAM. Can also be accessed relative to top of stack.
LOOP COUNTER	(32-bits, can decrement by 1) Used by class of test and loop instructions.
X REGISTER	(32-bits, can increment or decrement by 4). Used to point to RAM locations
PROGRAM COUNTER	(32-bits, increments by 4). Points to 4-byte instruction groups in RAM.
INSTRUCTION REG	(32-Bits). Holds 4-byte instruction groups while they are being decoded and executed.

* Math and logic operations use the TOP item and NEXT to top Parameter Stack items as the operands. The result is pushed onto the Parameter Stack.

* Return addresses from subroutines are placed on the Return Stack. The Y REGISTER is used as a pointer to RAM locations. Since the Y REGISTER is the top item of the Return Stack, nesting of indices is straightforward.
MODE—A register with mode and status bits

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MODE-BITS:

Slow down memory accesses by 8 if "1". Run full speed if "0" (Provided for access to slow EPROM)

Divide the system clock by 1023 if "1" to reduce power consumption. Run full speed if "0". (On-chip counters slow down if this bit is set)

Enable external interrupt 1.

Enable external interrupt 2.

Enable external interrupt 3.

Enable external interrupt 4.

Enable external interrupt 5.

Enable external interrupt 6.

Enable external interrupt 7.

ON-CHIP MEMORY LOCATIONS:

MODE-BITS

DMA-POINTER

DMA-COUNTER

STACK-POINTER—Pointer into Parameter Stack

STACK-DEPTH—Depth of on-chip Parameter Stack

RSTACK-POINTER—Pointer into Return Stack

RSTACK-DEPTH—Depth of on-chip Return Stack

ADDRESSING MODE HIGH POINTS

The data bus is 32-bits wide. All memory fetches and stores are 32-bits. Memory bus addresses are 30 bits. The least significant 2 bits are used to select one-of-four bytes in some addressing modes. The Program Counter, X Register and Y Register are implemented as D latches with their outputs going to the memory address bus and the bus increment/decrementer. Incrementing one of these registers can happen quickly because the incremented value has already rippled through the inc/dec logic and need only be clocked into the latch. Branches and Calls are made to 32-bit word boundaries.

INSTRUCTION SET

32-BIT INSTRUCTION FORMAT

The thirty two bit instructions are CALL, BRANCH, BRANCH-IF-ZERO and LOOP-IF-NOT-DONE. These instructions require the calculation of an effective address. In many computers, the effective address is calculated by adding or subtracting an operand with the current Program Counter. This math operation requires from four to seven machine cycles to perform and can definitely bog down machine execution. The microprocessor's strategy is to perform the required math operation at assembly or linking time and do a much simpler "Increment to next page" or "Decrement to previous page" operation at run time. As a result, the microprocessor branches execute in a single cycle.

24-BIT OPERAND FORM:

Byte 1 Byte 2 Byte 3 Byte 4

WWWWWW XX—YYYYYYYY—YYYYYYYY—
YYYYYYYY

With a 24-bit operand, the current page is considered to be defined by the most significant 6 bits of the Program Counter.

16-BIT OPERAND FORM:

QQQQQQQQ—WWWWWW XX—YYYYYYYY—
YYYYYYYY

With a 16-bit operand, the current page is considered to be defined by the most significant 14 bits of the Program Counter.

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8-BIT OPERAND FORM:

QQQQQQQQ—QQQQQQQQ—WWWWWW
XX—YYYYYYYY

With an 8-bit operand the current page is considered to be defined by the most significant 22 bits of the Program Counter.

QQQQQQQQ—Any 8-bit instruction

WWWWWW—Instruction op-code

XX—Select how the address bits will be used:

00—Make all high-order bits zero (Page zero addressing)

01—Increment the high-order bits (Use next page)

10—Decrement the high-order bits (Use previous page)

11—Leave the high-order bits unchanged (Use current page)

YYYYYYYY—The address operand field. This field is always shifted left two bits (to generate a word rather than byte address) and loaded into the Program Counter. The microprocessor instruction decoder figures out the width of the operand field by the location of the instruction op-code in the four bytes.

The compiler or assembler will normally use the shortest operand required to reach the desired address so that the leading bytes can be used to hold other instructions. The effective address is calculated by combining:

The current Program Counter

The 8, 16 or 24 bit address operand in the instruction.

Using one of the four allowed addressing modes.

EXAMPLES OF EFFECTIVE ADDRESS CALCULATION

EXAMPLE 1:

Byte 1	Byte 2	Byte 3	Byte 4
QQQQQQQQ	QQQQQQQQ	0000011	10011000

The "QQQQQQQQs" in Byte 1 and 2 indicate space in the 4-byte memory fetch which could be held two other instructions to be executed prior to the CALL instruction. Byte 3 indicates a CALL instruction (six zeros) in the current page (indicated by the 11 bits). Byte 4 indicates that the hexadecimal number 98 will be forced into the Program Counter bits 2 through 10. (Remember, a CALL or BRANCH always goes to a word boundary so the two least significant bits are always set to zero). The effect of this instruction would be to CALL a subroutine at WORD location HEX 98 in the current page. The most significant 22 bits of the Program Counter define the current page and will be unchanged.

EXAMPLE 2:

Byte 1	Byte 2	Byte 3	Byte 4
000001 01	00000001	00000000	00000000

If we assume that the Program Counter was HEX 0000 0156 which is binary:

00000000 00000000 00000001 01010110=OLD PROGRAM COUNTER.

Byte 1 indicates a BRANCH instruction op code (000001) and "01" indicates select the next page. Byte 2, 3, and 4 are the address operand. These 24-bits will be shifted to the left two places to define a WORD address. HEX 0156 shifted left two places is HEX 0558. Since this is a 24-bit operand instruction, the most significant 6 bits of the Program Counter define the current page. These six bits will be incremented to select the next page. Executing this instruc-

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tion will cause the Program Counter to be loaded with HEX 0400 0558 which is binary:

0000100 00000000 0000101 01011000 = NEW PROGRAM COUNTER.
INSTRUCTIONS
CALL-LONG
0000 00XXX - YYYYYYYY - YYYYYYYY - YYYYYYYY

Load the Program Counter with the effective WORD address specified. Push the current PC contents onto the RETURN STACK.

OTHER EFFECTS: CARRY or modes, no effect. May cause Return Stack to force an external memory cycle if on-chip Return Stack is full.

BRANCH

0000 01XX—YYYYYYYY—YYYYYYYY—
YYYYYYYY

Load the Program Counter with the effective WORD address specified.

OTHER EFFECTS: NONE

BRANCH-IF-ZERO

0000 10XX—YYYYYYYY—YYYYYYYY—
YYYYYYYY

Test the TOP value on the Parameter Stack. If the value is equal to zero, load the Program Counter with the effective WORD address specified. If the TOP value is not equal to zero, increment the Program Counter and fetch and execute the next instruction.

OTHER EFFECTS: NONE

LOOP-IF-NOT-DONE

0000 11YY—(XXXX XXXX)—(XXXX XXXX)—
(XXXX XXXX)

If the LOOP COUNTER is not zero load the Program Counter with the effective WORD address specified. If the LOOP COUNTER is zero, decrement the LOOP COUNTER, increment the Program Counter and fetch and execute the next instruction.

OTHER EFFECTS: NONE

8-BIT INSTRUCTIONS PHILOSOPHY

Most of the work in the microprocessor 50 is done by the 8-bit instructions. Eight bit instructions are possible with the microprocessor because of the extensive use of implied stack addressing. Many 32-bit architectures use 8-bits to specify the operation to perform but use an additional 24-bits to specify two sources and a destination.

For math and logic operations the microprocessor 50 exploits the inherent advantage of a stack by designating the source operand(s) as the top stack item and the next stack item. The math or logic operation is performed, the operands are popped from the stack, and the result is pushed back on the stack. The result is a very efficient utilization of instruction bits as well as registers. A comparable situation exists between Hewlett Packard calculators (which use a stack) and Texas Instrument calculators which don't. The identical operation on an HP will require one half to one third the keystrokes of the TI.

The availability of 8-bit instructions also allows another architectural innovation: the fetching of four instructions in a single 32-bit memory cycle. The advantages of fetching multiple instructions are:

Increased execution speed even with slow memories.

Similar performance to the Harvard (separate data and instruction busses) without the expense.

Opportunities to optimize groups of instructions.

The capability to perform loops within this mini-cache

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The microloops inside the four instruction group are effective for searches and block moves

SKIP INSTRUCTIONS

The microprocessor 50 fetches instructions in 32-bit chunks called 4-byte instruction groups. These four bytes may contain four 8-bit instructions or some mix of 8-bit and 16 or 24-bit instructions. SKIP instructions in the microprocessor skip any remaining instructions in a 4-byte instruction group and cause a memory fetch to get the next 4-byte instruction group. Conditional SKIPS when combined with 3-byte BRANCHES will create conditional BRANCHES. SKIPS may also be used in situations when no use can be made of the remaining bytes in a 4-instruction group. A SKIP executes in a single cycle whereas a group of three NOPs would take three cycles.

SKIP-ALWAYS—Skip any remaining instructions in this 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group.

SKIP-IF-ZERO—If the TOP item of the Parameter Stack is zero, skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte

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Microloops are a unique feature of the microprocessor architecture which allows controlled looping within a 4-byte instruction group. A microloop instruction tests the LOOP COUNTER for "0" and may perform an additional test. If the LOOP COUNTER is not "0" and the test is met, instruction execution continues with the first instruction in the 4-byte instruction group, and the LOOP COUNTER is decremented. A microloop instruction will usually be the last byte in a 4-byte instruction group, but it can be any byte. If the LOOP COUNTER is "0" or the test is not met, instruction execution continues with the next instruction. If the microloop is the last byte in the 4-byte instruction group, the most significant 30-bits of the Program Counter are incremented and the next 4-byte instruction group is fetched from memory. On a termination of the loop on LOOP COUNTER equal to "0", the LOOP COUNTER will remain at "0". Microloops allow short iterative work such as moves and searches to be performed without slowing down to fetch instructions from memory.

EXAMPLE:

Byte 1	Byte 2
FETCH-VIA-X-AUTOINCREMENT	STORE-VIA-Y-AUTOINCREMENT
Byte 3	Byte 4
LOOP-UNTIL-DONE	QQQQQQQQ

instruction group. If the TOP item is not zero, execute the next sequential instruction.

SKIP-IF-POSITIVE—If the TOP item of the Parameter Stack has a most significant bit (the sign bit) equal to "0", skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the TOP item is not "0", execute the next sequential instruction.

SKIP-IF-NO-CARRY—If the CARRY flag from a SHIFT or arithmetic operation is not equal to "1", skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the CARRY is equal to "1", execute the next sequential instruction.

SKIP-NEVER Execute the next sequential (NOP) instruction. (Delay one machine cycle).

SKIP-IF-NOT-ZERO—If the TOP item on the Parameter Stack is not equal to "0", skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the TOP item is equal "0", execute the next sequential instruction.

SKIP-IF-NEGATIVE—If the TOP item on the Parameter Stack has its most significant bit (sign bit) set to "1", skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the TOP item has its most significant bit set to "0", execute the next sequential instruction.

SKIP-IF-CARRY—If the CARRY flag is set to "1" as a result of SHIFT or arithmetic operation, skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the CARRY flag is "0", execute the next sequential instruction.

MICROLOOPS

This example will perform a block move. To initiate the transfer, X will be loaded with the starting address of the source. Y will be loaded with the starting address of the destination. The LOOP COUNTER will be loaded with the number of 32-bit words to move. The microloop will FETCH and STORE and count down the LOOP COUNTER until it reaches zero. QQQQQQQQ indicates any instruction can follow.

MICROLOOP INSTRUCTIONS

LOOP-UNTIL-DONE—If the LOOP COUNTER is not "0", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0", continue execution with the next instruction.

LOOP-IF-ZERO—If the LOOP COUNTER is not "0" and the TOP item on the Parameter Stack is "0", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the TOP item is "1", continue execution with the next instruction.

LOOP-IF-POSITIVE—If the LOOP COUNTER is not "0" and the most significant bit (sign bit) is "0", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the TOP item is "1", continue execution with the next instruction.

LOOP-IF-NOT-CARRY-CLEAR—If the LOOP COUNTER is not "0" and the floating point exponents found in TOP and NEXT are not aligned, continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the exponents are aligned, continue execution with the next instruction. This instruction is specifically designed for combination with special SHIFT instructions to align two floating point numbers.

LOOP-NEVER—(DECREMENT-LOOP-COUNTER) Decrement the LOOP COUNTER. Continue execution with the next instruction.

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ULOOP-IF-NOT-ZERO—If the LOOP COUNTER is not "0" and the TOP item of the Parameter Stack is "0", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the TOP item is "1", continue execution with the next instruction.

ULOOP-IF-NEGATIVE—If the LOOP COUNTER is not "0" and the most significant bit (sign bit) of the TOP item of the Parameter Stack is "1", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the most significant bit of the Parameter Stack is "0", continue execution with the next instruction.

ULOOP-IF-CARRY-SET—If the LOOP COUNTER is not "0" and the exponents of the floating point numbers found in TOP and NEXT are not aligned, continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the exponents are aligned, continue execution with the next instruction.

RETURN FROM SUBROUTINE OR INTERRUPT

Subroutine calls and interrupt acknowledgements cause a redirection of normal program execution. In both cases, the current Program Counter is pushed onto the Return Stack so the microprocessor can return to its place in the program after executing the subroutine or interrupt service routine.

NOTE: When a CALL to subroutine or interrupt is acknowledged the Program Counter has already been incremented and is pointing to the 4-byte instruction group following the 4-byte group currently being executed. The instruction decoding logic allows the microprocessor to perform a test and execute a return conditional on the outcome of the test in a single cycle. A RETURN pops an address from the Return Stack and stores it to the Program Counter.

RETURN INSTRUCTIONS

RETURN-ALWAYS—Pop the top item from the Return Stack and transfer it to the Program Counter.

RETURN-IF-ZERO—If the TOP item on the Parameter Stack is "0", pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-IF-POSITIVE—If the most significant bit (sign bit) of the TOP item on the Parameter Stack is a "0", pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-IF-CARRY-CLEAR—If the exponents of the floating point numbers found in TOP and NEXT are not aligned, pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-NEVER—Execute the next instruction (NOP)

RETURN-IF-NOT-ZERO—If the TOP item on the Parameter Stack is not "0", pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-IF-NEGATIVE—If the most significant bit (sign bit) of the TOP item on the Parameter Stack is a "1", pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-IF-CARRY-SET—If the exponents of the floating point numbers found in TOP and NEXT are aligned, pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

HANDLING MEMORY FROM DYNAMIC RAM

The microprocessor 50, like any RISC type architecture, is optimized to handle as many operations as possible

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on-chip for maximum speed. External memory operations take from 80 nsec. to 220 nsec. compared with on-chip memory speeds of from 4 nsec. to 30 nsec. There are times when external memory must be accessed.

External memory is accessed using three registers:

X-REGISTER—A 30-bit memory pointer which can be used for memory access and simultaneously incremented or decremented

Y-REGISTER—A 30-bit memory pointer which can be used for memory access and simultaneously incremented or decremented

PROGRAM-COUNTER—A 30-bit memory pointer normally used to point to 4-byte instruction groups. External memory may be accessed at addresses relative to the PC. The operands are sometimes called "Immediate" or "Literal" in other computers. When used as memory pointer the PC is also incremented after each operation.

MEMORY LOAD & STORE INSTRUCTIONS

FETCH-VIA-X—Fetch the 32-bit memory content pointed to by X and push it onto the Parameter Stack. X is unchanged.

FETCH-VIA-Y—Fetch the 32-bit memory content pointed to by Y and push it onto the Parameter Stack. Y is unchanged.

FETCH-VIA-X-AUTOINCREMENT—Fetch the 32-bit memory content pointed to by X and push it onto the Parameter Stack. After fetching, increment the most significant 30 bits of X to point to the next 32-bit word address.

FETCH-VIA-Y-AUTOINCREMENT—Fetch the 32-bit memory content pointed to by Y and push it onto the Parameter Stack. After fetching, increment the most significant 30 bits of Y to point to the next 32-bit word address.

FETCH-VIA-X-AUTODECREMENT—Fetch the 32-bit memory content pointed to by X and push it onto the Parameter Stack. After fetching, decrement the most significant 30 bits of X to point to the previous 32-bit word address.

FETCH-VIA-Y-AUTODECREMENT—Fetch the 32-bit memory content pointed to by Y and push it onto the Parameter Stack. After fetching, decrement the most significant 30 bits of Y to point to the previous 32-bit word address.

STORE-VIA-X—Pop the top item of the Parameter Stack and store it in the memory location pointed to by X. X is unchanged.

STORE-VIA-Y—Pop the top item of the Parameter Stack and store it in the memory location pointed to by Y. Y is unchanged.

STORE-VIA-X-AUTOINCREMENT—Pop the top item of the Parameter Stack and store it in the memory location pointed to by X. After storing, increment the most significant 30 bits of X to point to the next 32-bit word address.

STORE-VIA-Y-AUTOINCREMENT—Pop the top item of the Parameter Stack and store it in the memory location pointed to by Y. After storing, increment the most significant 30 bits of Y to point to the next 32-bit word address.

STORE-VIA-X-AUTODECREMENT—Pop the top item of the Parameter Stack and store it in the memory location pointed to by X. After storing, decrement the most significant 30 bits of X to point to the previous 32-bit word address.

STORE-VIA-Y-AUTODECREMENT—Pop the top item of the Parameter Stack and store it in the memory location pointed to by Y. After storing, decrement the most significant 30 bits of Y to point to the previous 32-bit word address.

FETCH-VIA-PC—Fetch the 32-bit memory content pointed to by the Program Counter and push it onto the Parameter

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Stack. After fetching increment the most significant 30 bits of the Program Counter to point to the next 32-bit word address.

*NOTE When this instruction executes, the PC is pointing to the memory location following the instruction. The effect is of loading a 32-bit immediate operand. This is an 8-bit instruction and therefore will be combined with other 8-bit instructions in a 4-byte instruction fetch. It is possible to have from one to four FETCH-VIA-PC instructions in a 4-byte instruction fetch. The PC increments after each execution of FETCH-VIA-PC, so it is possible to push four immediate operands on the stack. The four operands would be the found in the four memory locations following the instruction.

BYTE-FETCH-VIA-X—Fetch the 32-bit memory content pointed to by the most significant 30 bits of X. Using the two least significant bits of X, select one of four bytes from the 32-bit memory fetch, right justify the byte in a 32-bit field and push the selected byte preceded by leading zeros onto the Parameter Stack.

BYTE-STORE-VIA-X—Fetch the 32-bit memory content pointed to by the most significant 30 bits of X. Pop the TOP item from the Parameter Stack.

Using the two least significant bits of X place the least significant byte into the 32-bit memory data and write the 32-bit entity back to the location pointed to by the most significant 30 bits of X.

OTHER EFFECTS OF MEMORY ACCESS INSTRUCTIONS:

Any FETCH instruction will push a value on the Parameter Stack 74. If the on-chip stack is full, the stack will overflow into off-chip memory stack resulting in an additional memory cycle. Any STORE instruction will pop a value from the Parameter Stack 74. If the on-chip stack is empty, a memory cycle will be generated to fetch a value from off-chip memory stack.

HANDLING ON-CHIP VARIABLES

High-level languages often allow the creation of LOCAL VARIABLES. These variables are used by a particular procedure and discarded. In cases of nested procedures, layers of these variables must be maintained. On-chip storage is up to five times faster than off-chip RAM, so a means of keeping local variables on-chip can make operations run faster. The microprocessor 50 provides the capability for both on-chip storage of local variables and nesting of multiple levels of variables through the Return Stack.

The Return Stack 134 is implemented as 16 on-chip RAM locations. The most common use for the Return Stack 134 is storage of return addresses from subroutines and interrupt calls. The microprocessor allows these 16 locations to also be used as addressable registers. The 16 locations may be read and written by two instructions which indicate a Return Stack relative address from 0-15. When high-level procedures are nested, the current procedure variables push the previous procedure variables further down the Return Stack 134. Eventually, the Return Stack will automatically overflow into off-chip RAM.

ON-CHIP VARIABLE INSTRUCTIONS

READ-LOCAL-VARIABLE XXXX—Read the XXXXth location relative to the top of the Return Stack. (XXXX is a binary number from 0000-1111). Push the item read onto the Parameter Stack.

OTHER EFFECTS: If the Parameter Stack is full, the push operation will cause a memory cycle to be generated as one item of the stack is automatically stored to external RAM. The logic which selects the location performs a modulo 16 subtraction. If four local variables have been

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pushed onto the Return Stack, and an instruction attempts to READ the fifth item, unknown data will be returned.

WRITE-LOCAL-VARIABLE XXXX—Pop the TOP item of the Parameter Stack and write it into the XXXXth location relative to the top of the Return Stack. (XXXX is a binary number from 0000-1111).

OTHER EFFECTS: If the Parameter Stack is empty the pop operation will cause a memory cycle to be generated to fetch the Parameter Stack item from external RAM. The logic which selects the location performs a modulo 16 subtraction. If four local variables have been pushed onto the Return Stack, and an instruction attempts to WRITE to the fifth item, it is possible to clobber return addresses or wreak other havoc.

REGISTER AND FLIP-FLOP TRANSFER AND PUSH INSTRUCTIONS

DROP—Pop the TOP item from the Parameter Stack and discard it.

SWAP—Exchange the data in the TOP Parameter Stack location with the data in the NEXT Parameter Stack location.

DUP—Duplicate the TOP item on the Parameter Stack and push it onto the Parameter Stack.

PUSH-LOOP-COUNTER—Push the value in LOOP COUNTER onto the Parameter Stack.

POP-RSTACK-PUSH-TO-STACK—Pop the top item from the Return Stack and push it onto the Parameter Stack.

PUSH-X-REG—Push the value in the X Register onto the Parameter Stack.

PUSH-STACK-POINTER—Push the value of the Parameter Stack pointer onto the Parameter Stack.

PUSH-RSTACK-POINTER—Push the value of the Return Stack pointer onto the Return Stack.

PUSH-MODE-BITS—Push the value of the MODE REGISTER onto the Parameter Stack.

PUSH-INPUT—Read the 10 dedicated input bits and push the value (right justified and padded with leading zeros) onto the Parameter Stack.

SET-LOOP-COUNTER—Pop the TOP value from the Parameter Stack and store it into LOOP COUNTER.

POP-STACK-PUSH-TO-RSTACK—Pop the TOP item from the Parameter Stack and push it onto the Return Stack.

SET-X-REG—Pop the TOP item from the Parameter Stack and store it into the X Register.

SET-STACK-POINTER—Pop the TOP item from the Parameter Stack and store it into the Stack Pointer.

SET-RSTACK-POINTER—Pop the TOP item from the Parameter Stack and store it into the Return Stack Pointer.

SET-MODE-BITS—Pop the TOP value from the Parameter Stack and store it into the MODE BITS.

SET-OUTPUT—Pop the TOP item from the Parameter Stack and output it to the 10 dedicated output bits.

OTHER EFFECTS: Instructions which push or pop the Parameter Stack or Return Stack may cause a memory cycle as the stacks overflow back and forth between on-chip and off-chip memory.

LOADING A SHORT LITERAL

A special case of register transfer instruction is used to push an 8-bit literal onto the Parameter Stack. This instruction requires that the 8-bits to be pushed reside in the last byte of a 4-byte instruction group. The instruction op-code loading the literal may reside in ANY of the other three bytes in the instruction group.

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EXAMPLE:

BYTE 1	BYTE 2	BYTE 3
LOAD-SHORT-LITERAL	QQQQQQQQ	QQQQQQQQ
BYTE 4		
00001111		

In this example, QQQQQQQQ indicates any other 8-bit instruction. When Byte 1 is executed, binary 00001111 (HEX 0F) from Byte 4 will be pushed (right justified and padded by leading zeros) onto the Parameter Stack. Then the instructions in Byte 2 and Byte 3 will execute. The microprocessor instruction decoder knows not to execute Byte 4 it is possible to push three identical 8-bit values as follows:

BYTE 1	BYTE 2
LOAD-SHORT-LITERAL	LOAD-SHORT-LITERAL
BYTE 3	BYTE 4
LOAD-SHORT-LITERAL	00001111

SHORT-LITERAL-INSTRUCTION

LOAD-SHORT-LITERAL—Push the 8-bit value found in Byte 4 of the current 4-byte instruction group onto the Parameter Stack.

LOGIC INSTRUCTIONS

Logical and math operations use the stack for the source of one or two operands and as the destination for results. The stack organization is a particularly convenient arrangement for evaluating expressions. TOP indicates the top value on the Parameter Stack 74. NEXT indicates the next to top value on the Parameter Stack 74.

AND—Pop TOP and NEXT from the Parameter Stack, perform the logical AND operation on these two operands, and push the result onto the Parameter Stack.

OR—Pop TOP and NEXT from the Parameter Stack, perform the logical OR operation on these two operands and push the result onto the Parameter Stack.

XOR—Pop TOP and NEXT from the Parameter Stack, perform the logical exclusive OR on these two operands, and push the result onto the Parameter Stack.

BIT-CLEAR—Pop TOP and NEXT from the Parameter Stack, toggle all bits in NEXT, perform the logical AND operation on TOP, and push the result onto the Parameter Stack. (Another way of understanding this instruction is thinking of it as clearing all bits in TOP that are set in NEXT.)

MATH INSTRUCTIONS

Math instruction pop the TOP item and NEXT to top item of the Parameter Stack 74 to use as the operands. The results are pushed back on the Parameter Stack. The CARRY flag is used to latch the "33rd bit" of the ALU result.

ADD—Pop the TOP item and NEXT to top item from the Parameter Stack, add the values together and push the result back on the Parameter Stack. The CARRY flag may be changed.

ADD-WITH-CARRY—Pop the TOP item and the NEXT to top item from the Parameter Stack, add the values together. If the CARRY flag is "1" increment the result. Push the ultimate result back on the Parameter Stack. The CARRY flag may be changed.

ADD-X—Pop the TOP item from the Parameter Stack and read the third item from the top of the Parameter Stack. Add the values together and push the result back on the Parameter Stack. The CARRY flag may be changed.

SUB—Pop the TOP item and NEXT to top item from the Parameter Stack. Subtract NEXT from TOP and push the result back on the Parameter Stack. The CARRY flag may be changed.

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SUB-WITH-CARRY—Pop the TOP item and NEXT to top item from the Parameter Stack. Subtract NEXT from TOP. If the CARRY flag is "1" increment the result. Push the ultimate result back on the Parameter Stack. The CARRY flag may be changed.

SUB-X—

SIGNED-MULT-STEP—

UNSIGNED-MULT-STEP SIGNED-FAST-MULT—

FAST-MULT-STEP—

UNSIGNED-DIV-STEP—

GENERATE-POLYNOMIAL—

ROUND—

COMPARE—Pop the TOP item and NEXT to top item from the Parameter Stack. Subtract NEXT from TOP. If the result has the most significant bit equal to "0" (the result is positive), push the result onto the Parameter Stack. If the result has the most significant bit equal to "1" (the result is negative), push the old value of TOP onto the Parameter Stack. The CARRY flag may be affected.

SHIFT/ROTATE

SHIFT-LEFT—Shift the TOP Parameter Stack item left one bit. The CARRY flag is shifted into the least significant bit of TOP.

SHIFT-RIGHT—Shift the TOP Parameter Stack item right one bit. The least significant bit of TOP is shifted into the CARRY flag. Zero is shifted into the most significant bit of TOP.

DOUBLE-SHIFT-LEFT—Treating the TOP item of the Parameter Stack as the most significant word of a 64-bit number and the NEXT stack item as the least significant word, shift the combined 64-bit entity left one bit. The CARRY flag is shifted into the least significant bit of NEXT.

DOUBLE-SHIFT-RIGHT—Treating the TOP item of the Parameter Stack as the most significant word of a 64-bit number and the NEXT stack item as the least significant word, shift the combined 64-bit entity right one bit. The least significant bit of NEXT is shifted into the CARRY flag. Zero is shifted into the most significant bit of TOP.

OTHER INSTRUCTIONS

FLUSH-STACK—Empty all on-chip Parameter Stack locations into off-chip RAM. (This instruction is useful for multitasking applications.) This instruction accesses a counter which holds the depth of the on-chip stack and can require from none to 16 external memory cycles.

FLUSH-RSTACK—Empty all on-chip Return Stack locations into off-chip RAM. (This instruction is useful for multitasking applications.) This instruction accesses a counter which holds the depth of the on-chip Return Stack and can require from none to 16 external memory cycles.

It should further be apparent to those skilled in the art that various changes in form and details of the invention as shown and described may be made. It is intended that such changes be included within the spirit and scope of the claims appended hereto.

What is claimed is:

1. A microprocessor system comprising:

a central processing unit;

memory;

a bus connecting said central processing unit to said memory;

instruction fetching means that are connected to said bus to fetch instruction groups via said bus from said memory, certain of said instruction groups including at least one instruction that when executed, causes an access to an operand or an instruction or both, said operand or instruction being located a predetermined position from a boundary of said instruction groups;

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an instruction register for receiving sequential instructions from a first of said instruction groups from said instruction fetching means, said first of said instruction groups including said at least one instruction;

instruction decoding means having means for generating a counter control signal and an operand control signal; a counter that is connected to receive said counter control signal from said instruction decoding means;

operand selection means that is responsive to said operand control signal from said instruction decoding means;

instruction supplying means, responsive to said counter to select said predetermined position, for supplying, in succession from said instruction register, said sequential instructions to said central processing unit;

said instruction supplying means being further responsive to said counter and said operand selection means for selecting and supplying operand from said predetermined position in said instruction groups to said central processing unit;

said instruction decoding means providing said counter control signal and said operand control signal to cause said instruction supplying means to select from said instruction groups said operand or instruction or both associated with one of said instructions from said first of said instruction groups.

2 The microprocessor system of claim 1 wherein said instruction decoding means further includes means, responsive to a SKIP instruction in said instruction register, for configuring said instruction fetching means such that the next instruction group is supplied to the instruction register, and for configuring said instruction supplying means to supply in succession from said instruction register, said sequential instructions beginning with the first instruction in said instruction register from said next instruction group, to said central processing unit, and in which said means for generating counter control signal, also in response to the SKIP instruction, supplies the counter control signal to reset said counter to zero.

3 The microprocessor system of claim 2 further comprising:

means for determining whether a predefined condition exists within said microprocessor system and

means for controlling response of said instruction decoding means to said SKIP instruction and said predefined condition to execute or not execute said SKIP instruction based on existence of said predefined condition.

4 The microprocessor system of claim 1 further comprising:

a loop counter that is connected to receive a decrement control signal from said instruction decoding means, said instruction decoding means further including means, responsive to a MICROLOOP instruction in said instruction register, configured to supply said decrement control signal to said loop counter, said instruction supplying means being configured to supply from said instruction register beginning with the first instruction in said instruction register, from said first of said instruction groups, to said central processing unit, and in which said means for generating the counter control signal, also in response to the MICROLOOP instruction, supplies the counter control signal for resetting said counter to zero.

5 The microprocessor system of claim 4 further comprising:

means for determining whether a predefined condition exists within said microprocessor system and

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means for controlling response of said instruction decoding means to said MICROLOOP instruction and said predefined condition to execute or not execute said MICROLOOP instruction based on existence of said predefined condition.

6 The microprocessor system of claim 1 wherein said instruction decoding means includes means for supplying control signals to said instruction fetching means such that a subsequent one of said instruction groups is supplied to said instruction register, and for configuring said instruction supplying means to supply to said central processing unit a remainder of said first of said instruction groups as said operand.

7 The microprocessor system of claim 6 wherein said instruction decoding means are configured to supply control signals to said instruction fetching means such that a subsequent one of said instruction groups supplied to said instruction register is determined in response to a branch-type instruction in said sequential instructions within said first of said instruction groups.

8 The microprocessor system of claim 1 wherein said instruction decoding means configures said instruction supplying means to supply to said central processing unit a last byte of said first of said instruction groups as said operand in response to one of said sequential instructions within said first of said instruction groups.

9 The microprocessor system of claim 1 wherein said instruction decoding means are configured to supply control signals to said instruction fetching means such that a subsequent one of said instruction groups is supplied as an operand in response to one of said sequential instructions within said first of said instruction groups.

10 The microprocessor system of claim 1 wherein said instruction decoding means are configured to supply control signals to said instruction fetching means such that a subsequent one of said instruction groups supplied to said instruction register is determined in response to a branch-type instruction in said sequential instructions within said first of said instruction groups.

11 The microprocessor system of claim 10 in which said instruction decoding means supplies said counter control signal to reset said counter in response to a branch-type instruction in said sequential instructions within said first of said instruction groups.

12 The microprocessor system of claim 10 further comprising means for determining whether a predefined condition exists within said microprocessor system and

means for controlling response of said instruction decoding means to said branch-type instruction and said predefined condition to execute or not execute said branch-type instruction based on existence of said predefined condition.

13 The microprocessor system of claim 10 in which said instruction supplying means includes means for gating said sequential instructions within said instruction register to said central processing unit based on signals produced by said counter.

14 The microprocessor system of claim 1 wherein said instruction fetching means fetches said sequential instructions in parallel for each of said instruction groups in a single memory cycle.

15 The microprocessor system of claim 1 further comprising:

memory access testing means for testing said first of said instruction groups to determine if said sequential instructions require a memory access; and if said memory access testing means determine a memory access is not required, then supplying of control signals

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to said instruction fetching means to fetch the next instruction group during the execution of a current of said instruction groups

16. The microprocessor of claim 1 wherein said instruction supplying means includes:

- a decoder connected to an output of said counter, and
- a plurality of gates interposed between said instruction register and said central processing unit, said gates being controlled by signals from said decoder

17. The microprocessor of claim 1 wherein said instruction decoding means includes means for determining a width of said operand, said width being related to position in said instruction register of said one of said instructions of said first of said instruction groups.

18. The microprocessor of claim 1 wherein said first of said instruction groups includes a first instruction and multiple operand bytes, said instruction decoding means including means for determining a width of said operand associated with said first instruction based on position of said first instruction within said instruction register.

19. The microprocessor of claim 18 wherein said instruction supplying means includes gating means for selecting one or more of said multiple operand bytes within said instruction register corresponding to said operand.

20. A microprocessor comprising:

- a central processing unit;
- an instruction register operatively coupled to said central processing unit;
- instruction fetching means for providing sequential instructions within instruction groups to said instruction register wherein certain of said instruction groups include at least one instruction that, when executed, causes an access to an operand or an instruction or both, said operand or instruction being located at a predetermined position from a boundary of said instruction groups;
- instruction decoding means having a means for generating a counter control signal and an operand control signal;
- a counter that is connected to receive said counter control signal from said instruction decoding means;
- operand selection means that is responsive to said operand control signal from said instruction decoding means;
- instruction supplying means, responsive to said counter to select said predetermined position, for successively coupling said sequential instructions of said certain of said instruction groups to said central processing unit;
- said instruction supplying means being further responsive to said counter and said operand selection means for selection and supplying operands from said predetermined position in said instruction groups to said central processing unit; and
- said instruction decoding means providing said counter control signal and said operand control signal to cause said instruction supplying means to select from said instruction groups said operand or instruction or both associated with particular ones of said sequential instructions.

21. The microprocessor of claim 20 wherein said instruction decoding means, upon receiving a SKIP one of said sequential instructions from a current one of said instruction groups, configures said instruction fetching means to fetch a next one of said instruction groups to said instruction register supplies the counter control signal to reset said counter to zero and configures said instruction supplying means to supply a first one of said sequential instructions.

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22. The microprocessor of claim 21 further including means for determining whether a predefined condition exists within said microprocessor system, and

means for controlling response of said instruction decoding means to said SKIP instruction and said predefined condition to execute or not execute said SKIP instruction based on existence of said predefined condition.

23. The microprocessor of claim 20 further comprising a loop counter, said instruction decoding means, responsive to a MICROLOOP instruction within said instruction register, providing a decrement signal to said loop counter and providing the counter control signal to reset said counter to zero, and said instruction supplying means being configured to supply from said instruction register said sequential instructions, beginning with the first instruction in said instruction register, from a current one of said instruction groups, to said central processing unit.

24. The microprocessor of claim 23 further comprising: means for determining whether a predefined condition exists within said microprocessor system, and

means for controlling response of said instruction decoding means to said MICROLOOP instruction and said predefined condition to execute or not execute said MICROLOOP instruction based on existence of said predefined condition.

25. The microprocessor of claim 20 wherein said instruction decoding means includes means, responsive to ones of said sequential instructions of predetermined type, for supplying control signals to said instruction fetching means such that a subsequent one of said instruction groups is provided to said instruction register.

26. The microprocessor of claim 25 wherein said instruction decoding means includes means for configuring said instruction supplying means to supply a remainder of a current one of said instruction groups within said instruction register as said operand to said central processing unit.

27. The microprocessor of claim 25 further comprising means for determining whether a predefined condition exists within said microprocessor system, and means for controlling response of said instruction decoding means to branch-type ones of said instructions and said predefined condition to execute or not execute said branch-type ones of said instructions based on existence of said predefined condition.

28. The microprocessor of claim 20 wherein said instruction decoding means are configured to supply control signals to said instruction fetching means such that a subsequent one of said instruction groups is supplied as an operand in response to one of said sequential instructions.

29. In a microprocessor system including a central processing unit, memory, and an instruction register, a method for providing instructions and operands from said memory to said central processing unit comprising the steps of:

providing instruction groups to said instruction register from said memory wherein certain of said instruction groups include at least one instruction that, when executed, causes an access to an operand or an instruction or both, said operand or instruction being located at a predetermined position from a boundary of said instruction groups;

decoding said at least one instruction to determine said predetermined position;

locating said predetermined position; and

supplying, from said instruction groups, using the predetermined location, said operand or instruction or both to said central processing unit.

* * * * *

CIVIL COVER SHEET

no summons

The JS-44 civil cover sheet and the information contained herein neither replace nor supplement the filing and service of pleadings or other papers as required by law, except as provided by local rules of court. This form, approved by the Judicial Conference of the United States in September 1974, is required for the use of the Clerk of Court for the purpose of initiating the civil docket sheet. (SEE INSTRUCTIONS ON THE REVERSE OF THE FORM)

I. (a) PLAINTIFFS

Technology Properties Limited, Inc.,

(b) COUNTY OF RESIDENCE OF FIRST LISTED PLAINTIFF
(EXCEPT IN U.S. PLAINTIFF CASES)

(c) ATTORNEYS (FIRM NAME, ADDRESS, AND TELEPHONE NUMBER)

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DEFENDANTS

Fujitsu Limited, et al

COUNTY OF RESIDENCE OF FIRST LISTED DEFENDANT
(IN U.S. PLAINTIFF CASES ONLY)NOTE: IN LAND CONDEMNATION CASES USE THE LOCATION OF THE TRACT OF
LAND INVOLVED

ATTORNEYS (IF KNOWN)

2-05CV-494

II. BASIS OF JURISDICTION

(PLACE AN "X" IN ONE BOX ONLY)

- 1 U.S. Government Plaintiff ☒ 3 Federal Question (U.S. Government Not a Party)
- 2 U.S. Government Defendant 4 Diversity (Indicate Citizenship of Parties in Item III)

III. CITIZENSHIP OF PRINCIPAL PARTIES
(For Diversity Cases Only)(PLACE AN "X" IN ONE BOX FOR PLAINTIFF
AND ONE BOX FOR DEFENDANT)

	PTF	DEF		PTF	DEF
Citizen of This State	1	1	incorporated or Principal Place of Business in This State	4	4
Citizen of Another State	2	2	incorporated and Principal Place of Business in Another State	5	5
Citizen or Subject of a Foreign Country	3	3	Foreign Nation	6	6

IV. NATURE OF SUIT (PLACE AN "X" IN ONE BOX ONLY)

CONTRACT	TORTS	FORFEITURE/PENALTY	BANKRUPTCY	OTHER STATUTES
110 Insurance 120 Marine 130 Miller Act 140 Negotiable Instrument 150 Recovery of Overpayment & Enforcement of Judgment 151 Medicare Act 152 Recovery of Defaulted Student Loans (Excl. Veterans) 153 Recovery of Overpayment of Veteran's Benefits 160 Stockholders' Suits 190 Other Contract 195 Contract Product Liability	PERSONAL INJURY 310 Airplane 315 Airplane Product 320 Assault Libel & Slander 330 Federal Employers Liability 340 Marine 345 Marine Product Liability 350 Motor Vehicle 355 Motor Vehicle Product Liability 360 Other Personal Injury PERSONAL INJURY 362 Personal Injury - Med. Malpractice 365 Personal Injury - Product Liability 368 Asbestos Personal Injury Product Liability PERSONAL PROPERTY 370 Other Fraud 371 Truth in Lending 380 Other Personal Property Damage 385 Property Damage Product Liability	610 Agriculture 620 Other Food & Drug 625 Drug Related Seizure of Property 21 LISC 881 630 Liquor Laws 640 R.R. & Truck 650 Airline Regs. 660 Occupational Safety/Health 690 Other	422 Appeal 28 USC 158 423 Withdrawal 28 USC 157 PROPERTY RIGHTS 820 Copyrights X 830 Patent 840 Trademark SOCIAL SECURITY 861 HIA (1395ff) 862 Black Lung (923) 863 DIWC/DIWW (405(a)) 864 SSID Title XVI 865 RSI (405(g)) FEDERAL TAX SUITS 870 Taxes (U.S. Plaintiff or Defendant) 871 IRS - Third Party 26 USC 7609	400 State Reapportionment 410 Antitrust 430 Banks and Banking 450 Commerce/CC Rates/etc 460 Deportation 470 Racketeer Influenced and Corrupt Organizations 810 Selective Service 850 Securities/Commodities/Exchange 875 Customer Challenge 12 USC 3410 891 Agricultural Acts 892 Economic Stabilization Act 893 Environmental Matters 894 Energy Allocation Act 895 Freedom of Information Act 900 Appeal of Fee Determination Under Equal Access to Justice 950 Constitutionality of State Statutes 890 Other Statutory Actions
REAL PROPERTY 210 Land Condemnation 220 Foreclosure 230 Rent Lease & Ejectment 240 Torts to Land 245 Tort Product Liability 290 All Other Real Property	CIVIL RIGHTS 441 Voting 442 Employment 443 Housing Accommodations 444 Welfare 440 Other Civil Rights	PRISONER PETITIONS 510 Motions to Vacate Sentence HABEAS CORPUS: 530 General 535 Death Penalty 540 Mandamus & Other 550 Civil Rights 555 Prison Condition		

V. ORIGIN

(PLACE AN "X" IN ONE BOX ONLY)

- ☒ 1 Original Proceeding ☐ 2 Removed from State Court ☐ 3 Remanded from Appellate Court ☐ 4 Reinstated or Reopened ☐ 5 Transferred from another district (specify) ☐ 6 Multidistrict Litigation ☐ 7 Appeal to District Judge From Magistrate Judgment

VI. CAUSE OF ACTION (CITE THE U.S. CIVIL STATUTE UNDER WHICH YOU ARE FILING AND WRITE BRIEF STATEMENT OF CAUSE
DO NOT CITE JURISDICTIONAL STATUTES UNLESS DIVERSITY)

35 U.S.C. §§ 271 AND 283-285

VII. REQUESTED IN COMPLAINT:

CHECK IF THIS IS A CLASS ACTION UNDER FR C P 23 ☐

DEMAND \$

CHECK YES only if demanded in complaint:
JURY DEMAND: ☒ YES ☐ NOVII. RELATED CASE(S) (See Instructions):
IF ANY

DATE 10/24/05 SIGNATURE OF ATTORNEY OF RECORD S. Calvin Capshaw by permission et al

FOR OFFICE USE ONLY RECEIPT # MAG. JUDGE AMOUNT APPLYING IFP

EXHIBIT B

**TO THE DECLARATION OF JOHN L. COOPER IN
SUPPORT OF MOTION TO DISMISS AND TO
TRANSFER**

UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

TECHNOLOGY PROPERTIES LIMITED
and PATRIOT SCIENTIFIC CORPORATION,

Plaintiffs,

v.

MATSUSHITA ELECTRIC INDUSTRIAL
CO., LTD.; PANASONIC CORPORATION OF
NORTH AMERICA; JVC AMERICAS CORP.;
NEC ELECTRONICS AMERICA, INC.;
TOSHIBA CORPORATION; TOSHIBA
AMERICA, INC.; TOSHIBA AMERICA
ELECTRONIC COMPONENTS, INC.;
TOSHIBA AMERICA INFORMATION
SYSTEMS, INC.; and TOSHIBA AMERICA
CONSUMER PRODUCTS, LLC,

Defendants.

Civil Action No. 2-05CV-494 (TJW)

NOTICE OF FILING DEFENDANTS' TECHNOLOGY TUTORIAL

It is hereby certified that Defendants herein filed this Notice of Filing Technology
Tutorial on the 25th day of April, 2007.

April 25, 2007

Respectfully submitted on behalf of all Defendants,



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Toshiba America Electronic Components, Inc.;
Toshiba America Information Systems, Inc.; and
Toshiba America Consumer Products, LLC

CERTIFICATE OF SERVICE

The undersigned hereby certifies that all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3) this 25th day of April, 2007. Any other counsel of record will be served by facsimile transmission and/or first class mail.

A handwritten signature in black ink, appearing to read "Michael C. Smith", is written over a horizontal line.

Michael C. Smith

EXHIBIT C

**TO THE DECLARATION OF JOHN L. COOPER IN
SUPPORT OF MOTION TO DISMISS AND TO
TRANSFER**

**IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

TECHNOLOGY PROPERTIES LTD. and
PATRIOT SCIENTIFIC CORP.,
Plaintiffs,

vs.

MATSUSHITA ELECTRIC INDUSTRIAL
CO., LTD., ET AL.,
Defendants.

§ 100.00

CIVIL ACTION NO. 2:05-CV-494 (TJW)

MEMORANDUM OPINION AND ORDER

After considering the submissions and the arguments of counsel, the Court issues the following order concerning the claim construction issues:

I. Introduction

Plaintiffs Technology Properties Limited (“TPL”) and Patriot Scientific Corp. accuse multiple defendants of infringing United States Patent Nos. 5,809,336 (“the ‘336 patent”) entitled “High Performance Microprocessor Having Variable Speed System Clock,” 6,598,148 (“the ‘148 patent”) entitled “High Performance Microprocessor Having Variable Speed System Clock,” and 5,784,584 (“the ‘584 patent”) entitled “High Performance Microprocessor Using Instructions that Operate within Instruction Groups.” This opinion resolves the parties’ various claim construction disputes.

II. Background of the Technology

The '336 patent discloses a mechanism to improve the speed of microprocessor operations. First, a variable speed clock circuit is fabricated on the same chip as the microprocessor. By placing

the clock circuitry on the microprocessor, the clock will be subject to the same variations in operating conditions as the microprocessor. Second, the slower input/output clock is separated from the system clock.

The '148 patent also discloses a mechanism to improve the speed of the microprocessor. In addition to the on-chip clock described in the '336 patent, the microprocessor of the '148 patent includes memory on a majority of the microprocessor substrate.

The '584 patent addresses a bottleneck problem where the computing speed of the microprocessor depends on how quickly instructions can be loaded from memory into the instruction register of the microprocessor. Microprocessors can only process instructions as fast as the instructions can be loaded from the memory. The '584 patent discloses improvements on how to fetch and decode instructions. This is accomplished by arranging certain instructions into a group and fetching the entire group of instructions into the instruction register. As a result, the microprocessor no longer needs to wait for those instructions to be loaded from memory into the instruction register.

III. General Principles Governing Claim Construction

"A claim in a patent provides the metes and bounds of the right which the patent confers on the patentee to exclude others from making, using or selling the protected invention." *Burke, Inc. v. Bruno Indep. Living Aids, Inc.*, 183 F.3d 1334, 1340 (Fed. Cir. 1999). Claim construction is an issue of law for the court to decide. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 970-71 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370 (1996).

To ascertain the meaning of claims, the court looks to three primary sources: the claims, the specification, and the prosecution history. *Markman*, 52 F.3d at 979. Under the patent law, the

specification must contain a written description of the invention that enables one of ordinary skill in the art to make and use the invention. A patent's claims must be read in view of the specification, of which they are a part. *Id.* For claim construction purposes, the description may act as a sort of dictionary, which explains the invention and may define terms used in the claims. *Id.* "One purpose for examining the specification is to determine if the patentee has limited the scope of the claims." *Watts v. XL Sys., Inc.*, 232 F.3d 877, 882 (Fed. Cir. 2000).

Nonetheless, it is the function of the claims, not the specification, to set forth the limits of the patentee's claims. Otherwise, there would be no need for claims. *SRI Int'l v. Matsushita Elec. Corp.*, 775 F.2d 1107, 1121 (Fed. Cir. 1985) (en banc). The patentee is free to be his own lexicographer, but any special definition given to a word must be clearly set forth in the specification. *Intellicall, Inc. v. Phonometrics*, 952 F.2d 1384, 1388 (Fed. Cir. 1992). And, although the specification may indicate that certain embodiments are preferred, particular embodiments appearing in the specification will not be read into the claims when the claim language is broader than the embodiments. *Electro Med. Sys., S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 1054 (Fed. Cir. 1994).

This Court's claim construction decision must be informed by the Federal Circuit's decision in *Phillips v. AWH Corporation*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). In *Phillips*, the court set forth several guideposts that courts should follow when construing claims. In particular, the court reiterated that "the *claims* of a patent define the invention to which the patentee is entitled the right to exclude." 415 F.3d at 1312 (emphasis added) (*quoting Innova/Pure Water, Inc. v. Safari Water Filtration Systems, Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). To that end, the words used in a claim are generally given their ordinary and customary meaning. *Id.* The ordinary and customary

meaning of a claim term “is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application.” *Id.* at 1313. This principle of patent law flows naturally from the recognition that inventors are usually persons who are skilled in the field of the invention. The patent is addressed to and intended to be read by others skilled in the particular art. *Id.*

The primacy of claim terms notwithstanding, *Phillips* made clear that “the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification.” *Id.* Although the claims themselves may provide guidance as to the meaning of particular terms, those terms are part of “a fully integrated written instrument.” *Id.* at 1315 (quoting *Markman*, 52 F.3d at 978). Thus, the *Phillips* court emphasized the specification as being the primary basis for construing the claims. *Id.* at 1314-17. As the Supreme Court stated long ago, “in case of doubt or ambiguity it is proper in all cases to refer back to the descriptive portions of the specification to aid in solving the doubt or in ascertaining the true intent and meaning of the language employed in the claims.” *Bates v. Coe*, 98 U.S. 31, 38 (1878). In addressing the role of the specification, the *Phillips* court quoted with approval its earlier observations from *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998):

Ultimately, the interpretation to be given a term can only be determined and confirmed with a full understanding of what the inventors actually invented and intended to envelop with the claim. The construction that stays true to the claim language and most naturally aligns with the patent’s description of the invention will be, in the end, the correct construction.

Consequently, *Phillips* emphasized the important role the specification plays in the claim construction process.

The prosecution history also continues to play an important role in claim interpretation. The prosecution history helps to demonstrate how the inventor and the PTO understood the patent. *Phillips*, 415 F.3d at 1317. Because the file history, however, “represents an ongoing negotiation between the PTO and the applicant,” it may lack the clarity of the specification and thus be less useful in claim construction proceedings. *Id.* Nevertheless, the prosecution history is intrinsic evidence. That evidence is relevant to the determination of how the inventor understood the invention and whether the inventor limited the invention during prosecution by narrowing the scope of the claims.

Phillips rejected any claim construction approach that sacrificed the intrinsic record in favor of extrinsic evidence, such as dictionary definitions or expert testimony. The *en banc* court condemned the suggestion made by *Texas Digital Systems, Inc. v. Telegenix, Inc.*, 308 F.3d 1193 (Fed. Cir. 2002), that a court should discern the ordinary meaning of the claim terms (through dictionaries or otherwise) before resorting to the specification for certain limited purposes. *Id.* at 1319-24. The approach suggested by *Texas Digital*—the assignment of a limited role to the specification—was rejected as inconsistent with decisions holding the specification to be the best guide to the meaning of a disputed term. *Id.* at 1320-21. According to *Phillips*, reliance on dictionary definitions at the expense of the specification had the effect of “focus[ing] the inquiry on the abstract meaning of words rather than on the meaning of the claim terms within the context of the patent.” *Id.* at 1321. *Phillips* emphasized that the patent system is based on the proposition that the claims cover only the invented subject matter. *Id.* What is described in the claims flows from the statutory requirement imposed on the patentee to describe and particularly claim what he or she has invented. *Id.* The definitions found in dictionaries, however, often flow from the editors’

objective of assembling all of the possible definitions for a word. *Id.* at 1321-22.

Phillips does not preclude all uses of dictionaries in claim construction proceedings. Instead, the court assigned dictionaries a role subordinate to the intrinsic record. In doing so, the court emphasized that claim construction issues are not resolved by any magic formula. The court did not impose any particular sequence of steps for a court to follow when it considers disputed claim language. *Id.* at 1323-25. Rather, *Phillips* held that a court must attach the appropriate weight to the intrinsic sources offered in support of a proposed claim construction, bearing in mind the general rule that the claims measure the scope of the patent grant. The court now turns to a discussion of the relevant claim terms.

IV. Discussion

Claim 1 of the '336 patent, Claim 1 of the '148 patent, and Claim 29 of the '584 patent are representative of how the terms in dispute are used in the asserted claims. Claim 1 of the '336 patent is an independent apparatus claim. It provides:

A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.

Claim 1 of the '148 patent is an independent apparatus claim. It provides:

A microprocessor integrated circuit comprising:

a program-controlled processing unit operative in accordance with a sequence of program

instructions;

a memory coupled to said processing unit and capable of storing information provided by said processing unit;

a plurality of column latches coupled to the processing unit and the memory, wherein, during a read operation, a row of bits are read from the memory and stored in the column latch; and

a variable speed system clock having an output coupled to said processing unit;

said processing unit, said variable speed system clock, said plurality of column latches, and said memory fabricated on a single substrate, said memory using a greater area of said single substrate than said processing unit, said memory further using a majority of a total area of said single substrate.

Claim 29 of the '584 patent is a method claim. It provides:

In a microprocessor system including a central processing unit, memory, and an instruction register, a method for providing instructions and operands from said memory to said central processing unit comprising the steps of:

providing instruction groups to said instruction register from said memory wherein certain of said instruction groups include at least one instruction that, when executed, causes an access to an operand or an instruction or both, said operand or instruction being located at a predetermined position from a boundary of said instruction groups;

decoding said at least one instruction to determine said predetermined position;

locating said predetermined position; and

supplying, from said instruction groups, using the predetermined location, said operand or instruction or both to said central processing unit.

A. Agreed Construction

The parties have agreed to the construction of the following terms.

1. '336 Patent

"Oscillator" means "a circuit capable of maintaining an alternating output."

"On-chip input/output interface" means "a circuit having logic for input/output

communications, where that circuit is located on the same semiconductor substrate as the CPU (claims 1-2, 6-10) or the microprocessor (claims 3-5).”

“Integrated circuit” means “a miniature circuit on a single semiconductor substrate.”

“External memory bus” means “a group of conductors coupled between the I/O interface and an external storage device.”

2. ‘148 Patent

“Integrated circuit substrate” means “a single supporting material upon or within which is formed a miniature circuit.”

3. ‘584 Patent

“Instruction” means “a command to a processor that tells the processor what operation to perform.”

“Boundary of said instruction groups” means “beginning or end of an instruction group.”

“Supplying, from said instruction groups, using the predetermined location, said operand or instruction or both to said central processing unit” means “using the results of the locating step in the step of transferring the bits from the accessed operand or instruction to the central processing unit.”

“Instruction register” means “a hardware element that receives and holds an instruction group as it is extracted from memory; the register either contains or is connected to circuits that interpret the instructions in the group.”

B. Disputed Constructions

1. '336 Patent

a. "central processing unit"

The first term for construction is "central processing unit." The plaintiffs propose "an electronic circuit that controls the interpretation and execution of programmed instructions." The defendants propose "the central electronic circuit in a computer that controls the interpretation and execution of programmed instructions." There are two main disputes - 1) whether the circuit needs to be in a computer and 2) whether the circuit needs to be the "central electronic circuit."

In support of their construction, the plaintiffs argue that the specification teaches that the microprocessor can be used in applications other than a computer (e.g., HDTV and automobiles). '336 patent, 9:61-10:12. The plaintiffs also observe that the specification states that the microprocessor can be part of a multiprocessor system and, therefore, no one CPU is the "central electronic circuit" for the computer. *See* '336 patent, 11:64-12:4. The defendants, on the other hand, argue that they did not intend to limit the use of the CPU to a computer. They assert, however, that a CPU must be part of a computer chip.

The parties appear to agree that one of ordinary skill in the art would understand that a computer chip or other integrated circuit can be used in various devices, such as automobiles or televisions. The Court construes the term to mean "an electronic circuit on an integrated circuit that controls the interpretation and execution of programmed instructions."

b. "microprocessor"

The plaintiffs propose "an electronic circuit that executes programmed instructions and is capable of interfacing with input/output circuitry and/or memory circuitry." The defendants propose

“an electronic circuit that uses a central processing unit to interpret and execute programmed instructions.” The main disputes are whether the microprocessor must be capable of interfacing with input/output circuitry and/or memory circuitry, and whether the microprocessor needs to use a central processing unit.

The plaintiffs argue that the patent discloses a microprocessor that communicates with memory circuitry. ‘336 patent, 8:56-58, 11:49-54. The plaintiffs also argue that the claim language does not support the fact that a microprocessor is required to use a central processing unit because claim 3 does not recite the use of a central processing unit whereas all other independent claims require the use of a central processing unit.

The defendants argue that one of ordinary skill in the art would understand that microprocessors include a central processing unit. In addition, the defendants contend that not all microprocessors need to interface with input/output circuitry because some microprocessors communicate solely with external memory. The defendants also contend that microprocessors do not need to connect to external memory because some microprocessors rely solely on on-chip memory.

The Court is not persuaded that the additional limitations proposed by the plaintiffs or the defendants are appropriate. The input/output interface and the central processing unit limitations are included in other portions of the claims and, therefore, adding those limitations to the construction would be superfluous. *See, e.g.*, ‘336 patent, 32:12-13, 25-26. The Court construes “microprocessor” to mean “an electronic circuit that interprets and executes programmed instructions.”

c. “ring oscillator”

The next term is “ring oscillator.” The plaintiffs contend that this term means “an oscillator having a multiple, odd number of inversions arranged in a loop.” The defendants propose “an [oscillator] having an odd number of inverting logic stages connected in a loop.” The main dispute is whether a ring oscillator is required to have multiple inverters or whether it can have just one.

The plaintiffs argue that a single inverter would not be appropriate because it could not maintain an oscillating output. The defendants, on the other hand, rely on extrinsic evidence to support their proposed construction. Specifically, the defendants cite to a semiconductor textbook depicting a ring oscillator with only one inverter.

The plaintiffs have the better argument. The extrinsic evidence cited by the defendants also supports the plaintiffs’ construction. It states that timers are built as “chains of inverters,” not just one inverter. Defendants’ Claim Construction Brief, Ex. U, MEAD & CONWAY, INTRODUCTION TO VLSI SYSTEMS (1980), at 234. Accordingly, the Court adopts the plaintiffs’ proposed construction.

d. “an entire ring oscillator variable speed system clock in said integrated circuit”

The plaintiffs argue that this term means “a ring oscillator that generates the signal(s) used for timing the operation of the CPU, capable of operating at speeds that can change, where the ring oscillator is located entirely on the same semiconductor substrate as the CPU.” The defendants’ proposed construction is “a [ring oscillator variable speed system clock] that is completely on-chip and does not rely on a control signal or an external crystal/clock generator.” The dispute is whether the ring oscillator may rely on a control signal or an external crystal/clock generator.

In support of their construction, the defendants argue that the applicant disclaimed use of a

control signal and an external crystal/clock generator in order to distinguish over prior art. The plaintiffs contend that it did not disclaim all types of control signals, such as voltage and current controlled oscillators; there was only a disclaimer of the more narrow "command input." In addition, the plaintiffs argue that, although an external crystal is not directly used to generate a system clock signal, the external crystal can be used as a reference signal to account for delay across certain circuit elements.

The Court agrees with the defendants that the applicant disclaimed the use of an input control signal and an external crystal/clock generator to generate a clock signal. *See* Response to Office Action, April 11, 1996, at 8; Response to Office Action, January 13, 1997, at 4; Response to Office Action, July 7, 1997, at 3-4. Accordingly, the Court construes the term to mean "a ring oscillator variable speed system clock that is located entirely on the same semiconductor substrate as the CPU and does not directly rely on a command input control signal or an external crystal/clock generator to generate a clock signal."

e. "variable speed"

The next term is "variable speed." The plaintiffs' proposed construction is "capable of operating at speeds that can change." The defendants argue that the term means "a speed (frequency) that is not tightly controlled and varies more than minimally."

The plaintiffs contend that the specification discloses a ring oscillator that is capable of operating at various speeds based on variations in operating conditions. '336 patent, 16:59-63. The plaintiffs also argue that the defendants' proposed construction is too restrictive. The defendants, on the other hand, point to the prosecution where the applicant describes fixed-frequency as a speed that is "tightly controlled" and "var[ies] minimally." Amendment, July 7, 1997, at 3-4. According

to the defendants, “variable speed” is the opposite of fixed-frequency.

Notwithstanding the defendants’ arguments, one of ordinary skill in the art would understand “variable speed” to describe a component capable of operating at different speeds. Accordingly, the Court construes the term to mean “capable of operating at different speeds.”

f. “system clock” and “variable speed clock”¹

The plaintiffs propose “a circuit that generates the signal(s) used for timing the operation of the CPU.” The defendants contend that the term means “a circuit that is itself responsible for determining the frequency of the signal(s) used for timing the operation of the CPU.” The dispute is whether the circuit alone is responsible for determining the frequency of the signal.

A system clock does not generate the signal alone because the timing can be derived from the ring oscillator. ‘336 patent, 16:63-67. Accordingly, the Court adopts the plaintiffs’ proposed construction.

g. “oscillator . . . clocking”

The plaintiffs contend that no construction is necessary, but if a construction is required, they propose “the oscillator generates the signal(s) used for timing the operation of the CPU.” The defendants propose “an oscillator that is itself determining the frequency of the signal(s) used for timing.”

The Court agrees that the term requires construction. The Court construes the term to mean “an oscillator that generates the signal(s) used for timing the operation of the CPU.”

h. “processing frequency”

The plaintiffs propose “the speed at which the CPU operates.” The defendants propose

¹ The parties appear to agree that these two terms should have the same construction.

“fastest safe operating speed.” The issue is whether the term refers to the “fastest safe operating speed.”

The plaintiffs contend that the specification uses the language “maximum possible frequency” with regard to one embodiment of the CPU. The plaintiffs also point out that “fastest safe operating speed” was mentioned in response to an office action. Response to Office Action, January 8, 1997, at 4. The response to the office action states that the present invention provides

a variable speed clock for the microprocessor, with the clock speed varying in the same way as variations in the operating characteristics of the electronic devices making up the microprocessor. This allows the microprocessor to operate at its fastest safe operating speed, given its manufacturing process or changes in its operating temperature or voltage. *Id.* at 3-4.

According to the plaintiffs, this does not mean that the CPU must operate at the fastest safe operating speed, but that it is capable of operating at its fastest safe operating speed.

In support of their proposed construction, the defendants point to the specification which states that the “CPU will always execute at the maximum frequency possible, but never too fast.” ‘336 patent, 17:1-2. The defendants also point to a portion of the prosecution history which states that

these claims further state that the plurality of transistors included within the ring oscillator clock have operating characteristics which vary similarly to operating characteristics of transistors included within the microprocessor, thereby enabling the processing frequency of the microprocessor to track the speed of the ring oscillator clock: ‘...CPU clock 70 executes at the fastest speed possible using the adaptive ring counter clock 430. Speed may vary by a factor of four depending upon temperature, voltage, and process. Response to Office Action, April 11, 1996, at 8-9.

Frequency is not limited to the fastest safe operating speed. The portion of the prosecution history cited by the defendants refers to varying the processing frequency based on operating

conditions. In the Court's view, the applicants did not clearly define or limit the term "processing frequency." Accordingly, the Court adopts the plaintiffs' proposed construction.

i. "processing frequency capability"

The plaintiffs propose "the range of speeds at which the CPU can operate." The defendants propose "fastest safe operating speed at which the CPU can operate."

As discussed in the previous section, "processing frequency" is not limited to the "fastest safe operating speed." In addition, "capability" is not limited to a range or to the fastest speed. Accordingly, the Court construes the term to mean "the speeds at which the CPU can operate."

j. "varying together"²

The next term is "varying together." The plaintiffs contend that the term means "both increase or both decrease." The defendants' proposed construction is "increasing and decreasing by the same amount." The dispute is whether this term is limited to "the same amount."

The defendants claim that the only way for the invention to work is to match the clock speed to the CPU's processing speed capability. According to the defendants, if the frequency capability increased from 50 MHz to 100 MHz but the clock rate only increased from 25 MHz to 150 MHz, then the CPU would not be operable. In addition, the defendants argue that there are numerous statements in the prosecution history stating that the processing frequency should "track" or "vary correspondingly with" the clock rate. See Response to Office Action, April 11, 1996, at 6, 8; Response to Office Action, January 8, 1997, at 4.

There is no limitation in the intrinsic evidence requiring the variation between the frequency

² This construction would also include the terms "vary together," "varying . . . in the same way," and "varying in the same way."

capability and the clock to match exactly. The Court construes the term to mean “increasing and decreasing proportionally.”

k. “second clock”

The plaintiffs’ proposed construction is “a clock not derived from the first clock.” The defendants contend that no construction is necessary, but if construction is necessary, then they propose “another clock.”

The plaintiffs argue that the claims state that the second clock is independent of the first clock. According to the plaintiffs, a second clock derived from the first clock would not be independent as required by the claims.

The defendants appear to agree that the first clock is independent of the second clock. In any event, the independence of the second clock is required by the claim language. Accordingly, the Court declines to construe this term.

l. “external clock”

The plaintiffs propose “a clock not derived from the first clock, and which is not originated on the same semiconductor substrate upon which the entire variable speed clock is located.” The defendants contend that no construction is necessary, but if a construction is necessary, then they propose “a clock not on the integrated circuit substrate.”

As discussed previously, the defendants appear to agree that, like the second clock, the external clock is independent of the first clock. The plaintiffs’ proposed construction includes limitations already in the claims. The Court construes “external clock” to mean “a clock not on the integrated circuit substrate.”

**m. “second clock independent of said ring oscillator . . . system clock”
and “second clock independent of the ring oscillator system clock”**

The plaintiffs propose “a change in the frequency of the ring oscillator does not affect the frequency of the second clock.” The defendants propose “a second clock wherein a change in the frequency of one of the second clock or the ring oscillator system clock does not affect the frequency of the other.” The dispute is whether the term “independent” means “one-way independence” or “two-way independence.”

The plaintiffs argue that the specification only refers to one-way independence because it describes the situation where the I/O clock has a fixed speed while the CPU clock has a variable speed. According to the plaintiffs, there is no discussion about the situation where the I/O clock speed can be modified without affecting the CPU clock speed; the specification only states that varying the CPU clock speed would not affect the I/O clock speed.

The defendants argue that the plaintiffs’ construction would conflict with the purpose of the invention of having a first clock function independently from the second clock. According to the defendants, the specification describes the first and second clock as functioning independently from one another.

The defendants have the better argument. One of ordinary skill in the art would understand the term “independence” to mean “two-way independence.” Accordingly, the Court construes the term to mean “a second clock wherein a change in the frequency of either the second clock or ring oscillator system clock does not affect the frequency of the other.”

n. “external clock is operative at a frequency independent of a clock frequency of said oscillator”

The plaintiffs propose “a change in the frequency of the oscillator (claims 6-9) or the variable

speed clock (claim 10) does not affect the frequency of the external clock.” The defendants propose “an external clock wherein a change in the frequency of one of the external clock or oscillator does not affect the frequency of the other (claim 6).”

The Court construes the term to mean “an external clock wherein a change in the frequency of either the external clock or oscillator does not affect the frequency of the other.”

o. “fixed frequency”

The plaintiffs contend that no construction is necessary, but if the court determines that a construction is needed, then they propose “a non-variable frequency.” The defendants propose “having a speed that is tightly controlled and varies minimally.” This term is not a technical term and can be understood according to its plain and ordinary meaning. Accordingly, the Court declines to construe this term.

2. ‘148 Patent

a. “processing unit”

The plaintiffs propose “an electronic circuit that controls the interpretation and execution of programmed instructions.” The defendants do not appear to dispute the plaintiffs’ proposal. Accordingly, the Court adopts the plaintiffs’ proposed construction.

b. “memory” and “a memory”

The plaintiffs propose “all of the storage elements on the substrate and the control circuitry configured to access the storage elements.” The defendants claim that this term is indefinite, but if construction is possible, they propose “an information storing array that does not include registers,

cache or column latches.”³ The main dispute appears to be whether or not memory can include registers, cache, or column latches.

The defendants contend that “memory” and “column latches” must have different meanings because when two claim terms are used, they are presumed to mean different things. *See* ‘148 patent, claim 1. The defendants, therefore, argue that “memory” cannot include “column latches.” The defendants also point out that the specification recognizes that latches, registers and cache can exist within the CPU which is separate from the memory. *See* ‘148 patent, 4:5-10, 4:14-19, 5:58-60.

The plaintiffs contend that the specification describes DRAM to include registers and column latches. ‘148 patent, 8:65-9:4. The defendants, moreover, agree that registers, cache, and column latches may be considered part of the memory when they are included in the storage array. Defendants’ Responsive Claim Construction Brief, at 34.

In the Court’s view, the plaintiffs’ proposal is too broad because it would include storage elements that are within the CPU. On the other hand, the defendants’ proposed construction is too limiting because it would exclude registers and cache that one of ordinary skill in the art would consider to be types of memory. The claim language, however, does indicate that “memory” does not include “column latches.” “Memory” and “column latches” are two distinct elements in Claim 1 of the ‘148 patent. The claim also states, in relevant part, that “a plurality of column latches [is] coupled to . . . the memory” ‘148 patent, 31:11-12. If “memory” included “column latches,” then the claim would not need to specify that “column latches” are coupled to the “memory.” Accordingly, the Court construes “memory” to mean “storage elements other than column latches.”

³ The defendants do not present their arguments for indefiniteness in their claim construction briefing.

c. “total area of said single substrate” or “total area of said substrate”

The plaintiffs propose “the total surface of the supporting material upon or within which is formed an interconnected array of circuit elements.” The defendants propose “area enclosed by the outermost edges of the substrate.” This term is used in the context of memory which is claimed to occupy “a majority” of the “total area” of the substrate. The issue is what constitutes the “area.”

The plaintiffs argue that the defendants’ proposal would include areas of the substrate that are not being actively used (e.g., the sides and back of the substrate). According to the plaintiffs, the proper approach is to refer to the portion of the substrate that has active circuitry as depicted in Figure 9 of the ‘148 patent.

The area of the substrate refers to the top portion of the substrate, and not the sides or back. *See* ‘148 patent, Fig. 9. The Court construes the term to mean “the total top surface area of the substrate.”

d. “area of said single substrate” or “area of said substrate”

The Court construes this term to mean “the top surface area of the substrate.”

e. “variable”

This is not a technical term that requires construction and may be understood according to its plain and ordinary meaning. The Court declines to construe this term.

f. “system clock”

The Court adopts its previous construction of this term in the ‘336 patent. *See* Section IV(B)(1)(f).

g. “ring oscillator”

The Court adopts its previous construction of this term in the ‘336 patent. *See* Section IV(B)(1)(c).

h. “a ring oscillator having a variable output frequency”

The Court adopts its previous construction of “ring oscillator” in the ‘336 patent. *See* Section IV(B)(1)(c). No further construction of this term is necessary.

i. “the [ring oscillator] disposed on said integrated circuit substrate”

The Court adopts its previous construction of “ring oscillator” in the ‘336 patent. *See* Section IV(B)(1)(c). No further construction of this term is necessary.

j. “interface ports for interprocessor communication”

The plaintiffs contend that no construction is necessary. Alternatively, if a construction is needed, then the plaintiffs propose “channels through which data can be transferred between two separate processing units.” The defendants propose “channels through which data is transferred between two separate processing units.” The dispute is whether the interface ports may be used for purposes other than to transfer data.

The defendants argue that the plaintiffs’ construction would allow the interface ports to be used for any purpose and render the words “for interprocessor communication” meaningless. The plaintiffs contend that the specification describes interface ports for use other than interprocessor communication. *See* ‘148 patent, 9:64-10:12.

One of ordinary skill in the art would understand that interface ports are not limited solely to the transfer of data. The Court construes the term to mean “channels through which data is allowed to be transferred between two separate processing units.”

3. '584 Patent

a. "microprocessor"

The Court adopts its previous construction of this term in the '336 patent. *See* Section IV(B)(1)(b).

b. "central processing unit"

The Court adopts its previous construction of this term in the '336 patent. *See* Section IV(B)(1)(a).

c. "instruction groups"

The next term is "instruction groups." The plaintiffs' proposed construction is "sets of from 1 to a maximum number of sequential instructions, each set being provided to the instruction register as a unit and having a boundary." The defendants propose "sets of from 1 to a maximum number of sequential instructions, in which the execution of the instruction depends on each set being provided to the instruction register as a unit and in which any operand that is present must be right justified and which cannot encompass a single 32-bit traditional conventional instruction." The dispute is whether an operand that is present in the instruction group must be right justified and whether the instruction group may encompass a single 32-bit traditional conventional instruction.

The plaintiffs contend that right justified operands are a feature of the preferred embodiment. The plaintiffs also argue that the claim language was broadened during prosecution history when the language "selecting, in accordance with position in said instruction register of one of said instructions of one of said instruction groups, an operand from said one of said instruction groups" was removed from the claim. Amendment, June 12, 1997, at 6. In addition, the plaintiffs point out that the specification includes 32-bit instructions. *See* '584 patent, 20:41-42.

The defendants argue that the specification states that “operands must be right justified in the instruction register.” ‘584 patent, 16:15-16. In addition, the defendants argue that the applicants limited operands in this manner to overcome prior art rejections. *See* Amendment, June 17, 1997, at 13; Amendment, February 5, 1998, at 7. The defendants also contend that although the specification includes 32-bit instructions, the specification never identifies a *single* 32-bit instruction as instruction *groups*. According to the defendants, the specification defines “instruction group” as “being 8-bit and 16 or 24-bit instructions.” ‘584 patent, 23:4-7.

The specification and prosecution history refer to the fact that operands in the instruction register must be right justified. The applicants, however, did not exclude a single 32-bit instruction as an instruction group. In a preferred embodiment, a microprocessor fetches instructions “in 32-bit chunks called 4-byte instruction groups” where an “instruction group may contain from one to four instructions.” ‘584 patent, 23:4-5, 19:18-19. If a 4-byte (or 32-bit) instruction group contains one instruction, then the instruction group may contain a single 32-bit instruction. The Court construes “instruction groups” to mean “sets of from 1 to a maximum number of sequential instructions, each set being provided to the instruction register as a unit and having a boundary, and in which any operand that is present must be right justified.”

d. “operand”

The plaintiffs argue that the term means “an input to an operation specified by an instruction that is encoded as part of the instruction.” The defendants propose “an input to a single operation specified by an instruction that is encoded as part of the instruction where the size of the input can vary depending on the value of the input.”

The plaintiffs argue that the defendants’ proposed construction would exclude a preferred

embodiment which includes fixed length operands. See '584 patent, 29:62-27:7. However, the plaintiffs appear to agree that the size of the input can vary.

The intrinsic evidence does not show a clear limitation where the size of the input needs to vary depending on the value of the input. The Court construes the term to mean "an input to a single operation specified by an instruction that is encoded as part of the instruction where the size of the input can vary."

- e. **"said instruction groups include at least one instruction that, when executed, causes an access to an operand or instruction or both"**

The plaintiffs propose "the instruction being executed causes the CPU to use an immediate operand or execute a second instruction which is not the next sequential instruction." The defendants' proposed construction is "the instruction being executed causes the CPU to use data or execute a second instruction." The main dispute is whether the second instruction can be the next sequential instruction.

The plaintiffs argue that one of ordinary skill in the art would regard the normal program flow of going from one instruction to the next sequential instruction as "causing an access to an instruction." The defendants contend that the specification describes a SKIP instruction where the second instruction accessed is the next sequential instruction. '584 patent, 23:12-14. In reply, the plaintiffs contend that claim 29 refers to control flow instructions, not ordinary instructions.

The intrinsic evidence does not support the limitation proposed by the plaintiffs. Accordingly, the Court construes the term to mean "the instruction being executed causes the CPU to use an operand or execute a second instruction."

f. “said operand or instruction being located at a predetermined position from a boundary of said instruction groups”

The plaintiffs propose “the immediate operand or the instruction that is accessed has a position, relative to the beginning or end of the instruction group that includes the operand or instruction being accessed, that is determined based on a portion of an accessing instruction that identifies an operation to be performed and without reference to operand or address bits in the accessing instruction.” The defendants propose “the bits forming the accessed operand or instruction either begin or end at a position defined in relation to the boundaries of the instruction group in the instruction register rather than the currently executing instruction.” The principal dispute is whether the instruction group refers to the group in which the currently executing instruction is located or whether it refers to the group in which the instruction or operand being accessed is located.

The plaintiffs argue that, during prosecution, the applicants referred to the predetermined position of the *accessed* operand or instruction. *See* Supplemental Amendment, February 5, 1998, at 6-8. The plaintiffs also argue that instruction location is determined based on the particular place for instructions of that type. In addition, the plaintiffs contend that the target address specified by the instruction has no effect on the decision to begin executing at the beginning boundary of a target group.

The defendants argue that the Abstract explains the meaning of this phrase. It states

A high-performance microprocessor system using instruction that access operands and instructions located relative to the current instruction group rather than located relative to the current instructions, as is the convention, is disclosed herein. ‘584 patent, Abstract.

The defendants also contend that the plaintiffs add limitations that are not supported by the intrinsic evidence.

In reply, the plaintiffs contend that the term “current” in the Abstract refers to the target group, not the accessing group. For example, one of ordinary skill in the art would, in the case of a BRANCH instruction, determine the target instruction relative to the boundary of the target group, not the accessing group.

A “predetermined position” refers to a position based on the instruction group being accessed. *See* ‘584 patent, 2:29-35. The Court construes the term to mean “the operand or instruction is accessed at a position defined in relation to the boundaries of the instruction group that includes the operand or instruction being accessed.”

g. “decoding said at least one instruction to determine said predetermined position”

The plaintiffs contend that the term means “interpreting an instruction, in particular the portion thereof that signifies the operation to be performed, in order to identify a position relative to the beginning or end of the instruction group that includes the operand or instruction being accessed, without reference to the operand or address bits in the instruction being interpreted.” The defendants propose “interpreting an instruction, in particular the portion thereof that signifies the operation to be performed, in order to identify a position relative to the beginning or end of the current instruction group.”

The Court construes the term to mean “interpreting an instruction, in particular the portion therefor that signifies the operation to be performed, in order to identify a position relative to the beginning or end of the instruction group that includes the operand or instruction being accessed.”

h. “locating said predetermined position”

The next term is “locating said predetermined position.” The plaintiffs argue that this term

means “establishing operand or instruction supply within the instruction group that includes the operand or instruction being accessed at the predetermined position.” The defendants argue that the term means “using the results of the decoding step to ascertain the address of the accessed operand or instruction by referencing the current instruction group address rather than the current executing instruction address without adding or subtracting an operand with the current Program Counter.” The parties make similar arguments with regards to “predetermined position” as discussed in the previous section.

The plaintiffs oppose the additional limitation in the defendants’ proposed construction of “without adding or subtracting an operand with the current Program Counter.” According to the plaintiffs, this would exclude a preferred embodiment from the specification stating that the processor “treats the three operands similarly by adding or subtracting them to the current program counter.” ‘584 patent, 11:13-15. In support of this additional limitation, the defendants argue that additions and subtractions are done only at assembly/linking and not at run time. *See* ‘584 patent, 20:43-50.

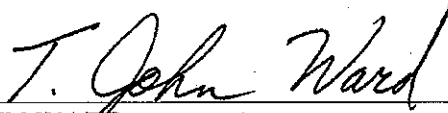
The defendants’ construction improperly incorporates a limitation from the preferred embodiment. The Court construes the term to mean “locating the operand or instruction within the instruction group that includes the operand or instruction being accessed at the predetermined position.”

V. Conclusion

The Court adopts the constructions set forth in this opinion for the disputed terms of the ‘336 patent, the ‘148 patent, and the ‘584 patent. The parties are ordered that they may not refer, directly or indirectly, to each other’s claim construction positions in the presence of the jury. Likewise, the parties are ordered to refrain from mentioning any portion of this opinion, other than the actual

definitions adopted by the Court, in the presence of the jury. Any reference to claim construction proceedings is limited to informing the jury of the definitions adopted by the Court.

SIGNED this 15th day of June, 2007.

A handwritten signature in black ink, reading "T. John Ward", is written over a horizontal line.

T. JOHN WARD
UNITED STATES DISTRICT JUDGE

EXHIBIT D

**TO THE DECLARATION OF JOHN L. COOPER IN
SUPPORT OF MOTION TO DISMISS AND TO
TRANSFER**

UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

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2007 OCT 22 PM 4:16
EASTERN-MARSHALL

Technology Properties Limited and Patriot
Scientific Corporation,

Plaintiffs,

v.

Matsushita Electrical Industrial Co., Ltd.,
Panasonic Corporation of North America, JVC
Americas Corporation, NEC Electronics
America, Inc., Toshiba Corporation, Toshiba
America, Inc., Toshiba America Electronic
Components, Inc., Toshiba America
Information Systems, Inc. and Toshiba America
Consumer Products, LLP, ARM Ltd. and ARM,
Inc.,

Defendants.

Case No. 2:05-CV-00494 (TJW)

BY _____


**PLAINTIFFS' AMENDED NOTICE OF APPEAL TO THE
UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT**

Plaintiffs, Technology Properties Limited and Patriot Scientific Corporation, hereby appeal from the Order and Partial Judgment of Non Infringement entered on September 12, 2007, in favor of defendants, ARM Ltd. and ARM, Inc., pursuant to Federal Rule of Civil Procedure 54(b). A copy of the Order is attached hereto.

This Amended Notice is filed to bring ARM Ltd. and ARM, Inc. into the case as appellees. Although noticed and served, these parties were inadvertently omitted from the case caption when the original Notice of Appeal was filed on September 27, 2007.

This Court has jurisdiction over this appeal under 28 U.S.C. section 1295.

DATED: October 22, 2007

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PATRIOT SCIENTIFIC CORPORATION**

CERTIFICATE OF SERVICE

I hereby certify that the following counsel of record who are deemed to have consented to electronic service are being served this 22nd day of October, 2007, with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3). Any other counsel of record will be served by electronic mail, facsimile transmission and/or first class mail on this same date


Elizabeth L. DeRieux

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

TECHNOLOGY PROPERTIES LTD, ET AL. §

Vs

§

CIVIL ACTION NO. 2:05-CV-494

MATSUSHITA ELECTRIC INDUS CO., §
LTD., ET AL

ORDER AND PARTIAL JUDGMENT OF NON-INFRINGEMENT

On this day came on to be heard Plaintiffs' and Defendants' Stipulation of Partial Judgment of Non-Infringement of U.S. Patent No. 5,784,584 ("the '584 patent") pursuant to F.R.C.P. 54(b). The court, after considering the Stipulation, finds that good cause exists and renders judgment as follows:

Pursuant to Federal Rule of Civil Procedure 54(b), this court finds that there is no just reason for delay and renders judgment in favor of all defendants of non-infringement of claim 29 of the '584 patent. In addition, the court finds that there is no just reason for delay and renders judgment in favor of defendants ARM Ltd. and ARM, Inc. (collectively "ARM") of non-infringement as to all claims asserted against ARM. Finally, although it is understood that the defendants have additional non-infringement arguments, invalidity arguments, equitable arguments, and other defenses and counterclaims, there is no need to reach these issues in view of the non-infringement judgment, and all counterclaims by the defendants with regard to declaratory judgment of alleged non-infringement, invalidity and/or unenforceability of the '584 patent are dismissed without prejudice.

All parties shall bear their own attorneys fees and costs

The clerk of court shall enter partial judgment in accordance herewith.

Baker-Lehne, Susan

From: txedCM@txed.uscourts.gov
Sent: Wednesday, September 12, 2007 1:02 PM
To: txedcmcc@txed.uscourts.gov
Subject: Activity in Case 2:05-cv-00494-TJW Technology Properties Limited, Inc v Fujitsu Limited et al
"Order"

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U.S. District Court [LIVE]

Eastern District of TEXAS LIVE

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Case Name: Technology Properties Limited, Inc , v Fujitsu Limited et al

Case Number: 2:05-cv-494

Filer:

Document Number: 314

Docket Text:

ORDER - granting [294] Pla and Dft Stipulation of Partial Judgment of Non-Infringement of US Patent No 5,784,584 pursuant to F. R. C. P 54 (b) The court renders judgment as follows herein Signed by Judge T. John Ward on 9/12/07 (ch,)

The following document(s) are associated with this transaction:

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[STAMP dcecfStamp_ID=1041545818 [Date=9/12/2007] [FileNumber=1949843-0]
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614e29bf54a9390610887adc232bb56684716078d8cbc4c7f5004f272321d]]

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2:05-cv-494 Notice will be delivered by other means to:

EXHIBIT E

**TO THE DECLARATION OF JOHN L. COOPER IN
SUPPORT OF MOTION TO DISMISS AND TO
TRANSFER**

**UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

Technology Properties Limited, Inc., and Patriot Scientific Corporation,

Plaintiffs,

v.

Fujitsu Limited, Fujitsu General America, Inc.,
Fujitsu Computer Products of America, Inc.,
Fujitsu Computer Systems Corp., Fujitsu
Microelectronics America, Inc., Fujitsu Ten
Corporation of America, Matsushita Electrical
Industrial Co., Ltd., Panasonic Corporation of
North America, JVC Americas Corporation,
NEC Corporation, NEC Electronics America,
Inc., NEC America, Inc., NEC Display
Solutions of America, Inc., NEC Solutions
America, Inc., NEC Unified Solutions, Inc.,
Toshiba Corporation, Toshiba America, Inc.,
Toshiba America Electronic Components, Inc.,
Toshiba America Information Systems, Inc.,
Toshiba America Consumer Products, LLC., ARM, Ltd.,
and ARM, Inc.

Defendants

2:05-cv-00494-TJW

**FIRST AMENDED ANSWER OF ARM, LTD. AND ARM, INC. TO PLAINTIFFS'
SECOND AMENDED COMPLAINT FOR PATENT INFRINGEMENT**

Defendants-Intervenors ARM, Ltd. and ARM, Inc. (collectively, "ARM") by and through its undersigned counsel, hereby present its Answer and Defenses to Plaintiffs Technology Properties Limited ("TPL") and Patriot Scientific Corporation's ("Patriot") (collectively "Plaintiffs") Second Amended Complaint for Patent Infringement (the "Complaint"), filed February 2, 2007. All Paragraph references refer to the corresponding paragraph in the Complaint.

PARTIES

1. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 1, and therefore denies same.

2. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 2, and therefore denies same.

3. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 3, and therefore denies same.

4. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 4, and therefore denies same.

5. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 5, and therefore denies same.

6. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 6, and therefore denies same.

7. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 7, and therefore denies same.

8. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 8, and therefore denies same.

9. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 9, and therefore denies same.

10. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 10, and therefore denies same.

11. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 11, and therefore denies same.

12. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 12, and therefore denies same.

13. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 13, and therefore denies same.

14. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 14, and therefore denies same.

15. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 15, and therefore denies same.

16. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 16, and therefore denies same.

17. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 17, and therefore denies same.

18. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 18, and therefore denies same.

19. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 19, and therefore denies same.

20. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 20, and therefore denies same.

21. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 21, and therefore denies same.

22. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 22, and therefore denies same.

JURISDICTION AND VENUE

23. Paragraph 23 contains conclusions of law and not averments of fact to which an answer is required, but insofar as an answer may be deemed required, ARM admits that based only on the allegations in the Complaint, this action likely arises under the patent laws of the United States, 35 U.S.C. § 1, *et seq.* and that under 28 U.S.C. § 1338(a), the Court has original jurisdiction over civil actions arising under the patent laws.

24. Paragraph 24 contains conclusions of law and not averments of fact to which an answer is required, but insofar as an answer may be deemed required, ARM denies that it has committed acts of infringement or continues to commit acts of infringement anywhere and admits that based only on the allegations in the Complaint, venue appears to be proper in this Court under 28 U.S.C. §§ 1391(c) and 1400(b).

THE PATENTS

25. ARM admits that United States Patent No. 6,598,148 (the “‘148 patent”) states as its title “High Performance Microprocessor Having Variable Speed System Clock” and that Exhibit A to the Complaint appears to be a copy of the ‘148 patent. ARM is without knowledge or information sufficient to form a belief as to the remaining averments of Paragraph 25, and therefore denies same.

26. ARM admits that United States Patent No. 5,809,336 (the “‘336 patent”) states as its title “High Performance Microprocessor Having Variable Speed System Clock” and that Exhibit B to the Complaint appears to be a copy of the ‘336 patent. ARM is without knowledge or information sufficient to form a belief as to the remaining averments of Paragraph 26, and therefore denies same.

27. ARM admits that United States Patent No. 5,784,584 (the “‘584 patent”) states as its title “High Performance Microprocessor Using Instructions That Operate Within Instruction

Groups” and that Exhibit C to the Complaint appears to be a copy of the ‘584 patent. ARM is without knowledge or information sufficient to form a belief as to the remaining averments of Paragraph 27, and therefore denies same.

28. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 28, and therefore denies same.

29. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 29, and therefore denies same.

30. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 30, and therefore denies same.

ALLEGED INFRINGEMENT BY FUJITSU

31. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 31, and therefore denies same.

32. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 32, and therefore denies same.

33. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 33, and therefore denies same.

34. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 34, and therefore denies same.

35. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 35, and therefore denies same.

36. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 36, and therefore denies same.

37. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 37, and therefore denies same.

38. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 38, and therefore denies same.

39. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 39, and therefore denies same.

40. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 40, and therefore denies same.

41. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 41, and therefore denies same.

42. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 42, and therefore denies same.

43. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 43, and therefore denies same.

44. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 44, and therefore denies same.

45. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 45, and therefore denies same.

46. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 46, and therefore denies same.

47. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 47, and therefore denies same.

48. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 48, and therefore denies same.

ALLEGED INFRINGEMENT BY MATSUSHITA

49. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 49, and therefore denies same.

50. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 50, and therefore denies same.

51. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 51, and therefore denies same.

52. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 52, and therefore denies same.

53. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 53, and therefore denies same.

54. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 54, and therefore denies same.

55. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 55, and therefore denies same.

56. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 56, and therefore denies same.

57. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 57, and therefore denies same.

ALLEGED INFRINGEMENT BY NEC

58. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 58, and therefore denies same.

59. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 59, and therefore denies same.

60. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 60, and therefore denies same.

61. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 61, and therefore denies same.

62. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 62, and therefore denies same.

63. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 63, and therefore denies same.

64. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 64, and therefore denies same.

65. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 65, and therefore denies same.

66. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 66, and therefore denies same.

67. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 67, and therefore denies same.

68. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 68, and therefore denies same.

69. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 69, and therefore denies same.

70. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 70, and therefore denies same.

71. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 71, and therefore denies same.

72. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 72, and therefore denies same.

73. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 73, and therefore denies same.

74. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 74, and therefore denies same.

75. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 75, and therefore denies same.

ALLEGED INFRINGEMENT BY TOSHIBA

76. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 76, and therefore denies same.

77. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 77, and therefore denies same.

78. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 78, and therefore denies same.

79. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 79, and therefore denies same.

80. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 80, and therefore denies same.

81. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 81, and therefore denies same.

82. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 82, and therefore denies same.

83. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 83, and therefore denies same.

84. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 84, and therefore denies same.

85. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 85, and therefore denies same.

86. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 86, and therefore denies same.

87. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 87, and therefore denies same.

88. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 88, and therefore denies same.

89. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 89, and therefore denies same.

90. ARM is without knowledge or information sufficient to form a belief as to the averments of Paragraph 90, and therefore denies same.

PLAINTIFFS' PRAYER FOR RELIEF

91. ARM denies that Plaintiffs are entitled to any of the relief stated in Plaintiffs' Prayer for Relief.

92. All remaining averments not specifically admitted herein are denied.

ARM SPECIFIC AVERMENTS

93. ARM, Ltd. is a subsidiary of ARM Holdings plc and a corporation organized under the laws of the England and Wales, with its principal place of business in Cambridge, England.

94. ARM, Inc. is a subsidiary of ARM Holdings plc and a corporation organized under the laws of California, with its principal place of business in Sunnyvale, California.

DEFENSE AND AFFIRMATIVE DEFENSES

95. The claims of the '584 patent are invalid and/or unenforceable under one or more provisions of Title 35, United States Code, including without limitation, §§ 102, 103, and/or 112 thereof.

96. ARM has not committed any act that would give rise to liability for infringement of any properly construed, valid claim of the '584 patent.

97. Plaintiffs do not have the requisite ownership rights to establish standing to sue as to the '584 patent.

98. All or some of Plaintiffs' claims are barred by the doctrine of laches.

99. All or some of Plaintiffs' claims are barred by equitable estoppel.

100. The Complaint fails to state a claim upon which relief can be granted.

101. Plaintiffs' asserted damages are limited by 35 U.S.C. § 287.

102. Plaintiffs' claims for infringement of the '584 patent are barred because those patents are unenforceable and/or invalid as a result of inequitable conduct and/or failure to name the proper inventors.

a. Two individuals, Mr. Charles Moore and Mr. Russell Fish, are named as inventors on the face of the '584 patent.

b. In late 1988, Mr. Moore had previous experience designing Forth-based microprocessors, while Mr. Fish had experience in sales and marketing of microprocessors.

c. During 1989, Mr. Moore utilized the Semiconductor Design Center of Japanese semiconductor manufacturer, Oki, in Sunnyvale, California, to carry out his microprocessor design activities. Mr. Fish did not have access to the Oki Design Center.

d. During the time before the filing of U.S. Patent Application No. 07/389,334 (the "Application"), divisions of which issued as the '584 patent, Mr. Moore worked on designing the microprocessor discussed in the Application. Mr. Fish, however, worked on marketing that microprocessor. Mr. Fish was not concerned about the problems addressed by the microprocessor design disclosed in the Application.

e. Mr. Moore did all the design work on the microprocessor disclosed in the Application by himself.

f. None of the persons substantially involved in the prosecution of the Application, including Mr. Moore and Mr. Fish, disclosed to the patent office that Mr. Moore had performed all of the design work on the disclosed microprocessor himself.

g. Mr. Moore and Mr. Fish submitted declarations signed under oath stating that Mr. Fish was an inventor of the subject matter claimed in the Application.

h. Mr. Fish did none of the design work on the disclosed microprocessor. Mr. Fish was only responsible for marketing and potential sales of the microprocessor.

i. Mr. Fish was not an inventor of the subject matter claimed in the Application.

j. The misstatements made by both Mr. Moore and Mr. Fish that Mr. Fish was an inventor were material.

k. Mr. Moore was motivated to state that Mr. Fish was an inventor because he wanted to convince Mr. Fish to make every effort to market the microprocessor that Mr. Moore had designed.

l. Mr. Fish was motivated to claim inventorship both to receive a share of any patent rights that might result from the Application and for the recognition of being an inventor.

m. At least Mr. Moore was aware that Mr. Fish was not an inventor and intended to deceive the patent office when he declared under penalty of perjury that Mr. Fish was an inventor.

103. ARM reserves the right to offer additional defenses that cannot now be articulated due to the need for further discovery regarding Plaintiffs' claims.

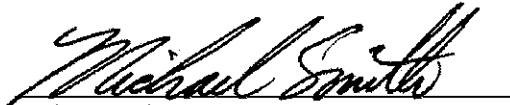
PRAYER FOR RELIEF

WHEREFORE, ARM prays for judgment that:

1. Plaintiffs be denied all relief and take nothing;
2. Judgment be entered that ARM has not, and does not, infringe, directly or indirectly, any properly construed, valid enforceable claim of the '584 patent;
3. Judgment be entered that the '584 patent is invalid and/or unenforceable;
4. This case be declared exceptional pursuant to 35 U.S.C. § 285 and that this Court award ARM the costs of this action, including reasonable attorneys' fees and litigation expenses;
5. ARM be awarded such other and further relief as the Court deems just and proper.

A JURY TRIAL IS DEMANDED AS TO ALL ELEMENTS TRIABLE BY JURY.

Respectfully submitted,



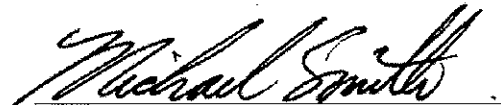
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Fax: (202) 719-7049

COUNSEL FOR ARM LTD. AND ARM, INC.

CERTIFICATE OF SERVICE

The undersigned hereby certifies that all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3) this 16th day of February, 2007. Any other counsel of record will be served by facsimile transmission and/or first class mail.



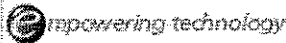
Michael C. Smith

EXHIBIT F

**TO THE DECLARATION OF JOHN L. COOPER IN
SUPPORT OF MOTION TO DISMISS AND TO
TRANSFER**



United States



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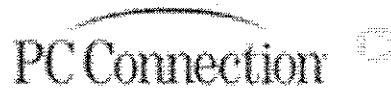
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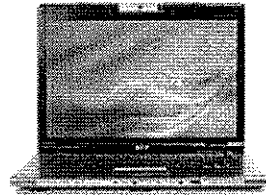
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25.



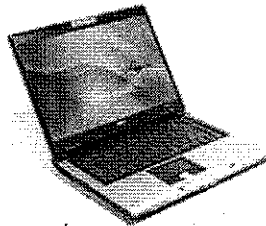
**Acer TravelMate 8210-6632
15.4" Laptop (Intel Core 2 Duo
Processor, 2 GB RAM, 160 GB
Hard Drive, Blue-Ray DVD Drive,
Vista Ultimate)**

Available at external website:
[TheNerds.net](#) for **\$2,160.99**

Product Details

- 2 GHz
- 2000 MB DDR2 SDRAM

28.



**Acer Aspire AS56806516 15.4"
Laptop (Intel Core 2 Duo
Processor T5500, 2 GB RAM, 120
GB Hard Drive, Super-Multi
drive)**

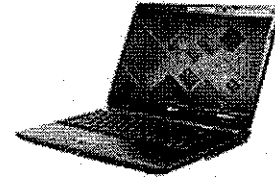
Currently unavailable

☆☆☆☆☆ (1)

Product Details

- 1.66 GHz

26.



**Acer TravelMate 4720-6220
14.1" Laptop (2 GHz Intel
Centrino Duo T7300 Processor,
GB RAM, 120 GB Hard Drive,
Vista Business)**

Buy new: \$899.00

6 Used & new from \$883.10

In Stock

Eligible for **FREE** Super Saver Shipping

Product Details

- 2 GHz

29.



**Acer TravelMate 6460-6263
15.4" Laptop (Intel Core 2 Duo
Processor, 2 GB RAM, 160 GB
Hard Drive, DVD Drive, Vista
Business)**

Buy new: \$1,699.00

Usually ships in 1 to 3 weeks

Eligible for **FREE** Super Saver Shipping

☆☆☆☆☆ (1)

Product Details

Price

Any Price

\$200-\$499 (5)
\$500-\$999 (56)
\$1000-\$1999 (18)
\$2000-\$4999 (3)

\$ to \$

CPU Speed

Any CPU Speed

1.5 GHz & Under (2)
1.6 to 1.9 GHz (33)
2 to 2.9 GHz (16)

Computer Platform

Any Computer Platform

PC (54)

• 2 GHz

Display Size

Any Display Size

- 10 to 13 in. (3)
- 14 to 15 in. (44)
- 16 to 17 in. (5)
- 20 to 29 in. (1)

Shipping Option

Any Shipping Option

Can be shipped within one business day from Amazon.com (2)

Related Categories

Bluetooth

New Arrivals

31.



Acer TravelMate 8210-6038 15.4" Laptop (Intel Core 2 Duo Processor, 2 GB RAM, 160 GB Hard Drive, Blu-Ray DVD Drive)

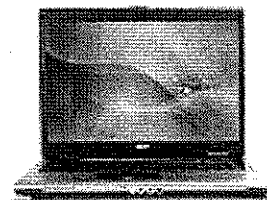
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★★★★☆ (4)

Product Details

- 2.16 GHz
- 2000 MB DDR2 SDRAM

32.

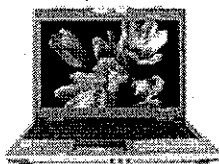


Acer Aspire AS51005033 15.4" Laptop (AMD Turion 64 X2 Mobile Processor, 1 GB RAM, 120 GB Hard Drive, DVD Drive, Vista Premium)

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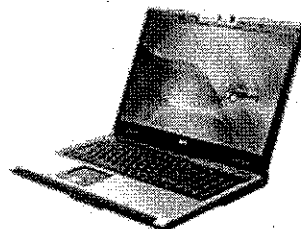
★★★★☆ (11)

34.



Acer Aspire 5050-5430 14.1" Laptop Computer (AMD Athlon 64 X2 Dual-Core TK-53, 1 GB RAM, 120 GB Hard Drive, Dual-Layer DVD-RW, WXGA, Windows Vista Home Premium)

2 Used & new from \$619.99



Acer AS93005005 17" Laptop (AMD Turion 64 X2 Mobile Processor, 1 GB RAM, 120 GB Hard Drive, DVD Drive, Vista Home Premium)

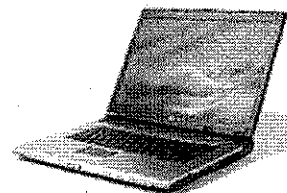
Currently unavailable

★★★★☆ (3)

Product Details

- 1.6 GHz

35.



Acer TravelMate 4200-4091 15.4" Laptop (Intel Core Duo Processor, 1 GB RAM, 120 GB Hard Drive, DVD Drive, Vista Business)

Sign up to be notified when this item becomes available.

Product Details

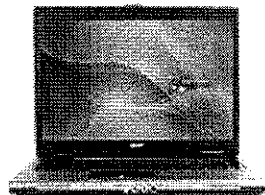
- 1.66 GHz

37.



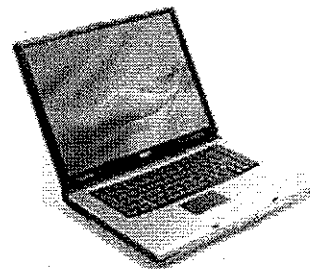
Acer Aspire Celeron 1.73GHz 512MB 80GB CDRW/DVD 14.1" Vista

Buy new: \$534.79
In Stock



Acer Aspire AS31001868 15.4" Laptop (AMD Sempron 3400+ Processor, 512 MB RAM, 80 GB Hard Drive, DVD Drive, Vista)

38.



Acer TM42306499 15.4" Laptop (Intel Core 2 Duo Processor, 1 GB RAM, 120 GB Hard Drive, DVD Drive, Vista Business)

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GEEK Stuff: A list by Mack
D. Land "Wizard55" ☒



Things i want!: A list by
Robert Persico "TJP" ☒

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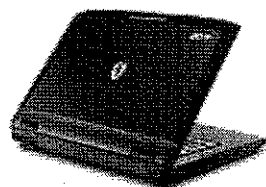
Currently unavailable

★★★★★ (1)

Product Details

• 1.8 GHz

40.



Acer Ferrari 1000-5123 12.1" Laptop (AMD 64 X2 Mobile Processor, 2 GB RAM, 160 GB Hard Drive, DVD Drive, Vista Ultimate)

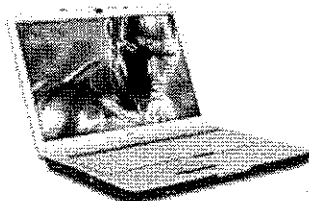
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★★★★★ (1)

Product Details

• 1.8 GHz

43.

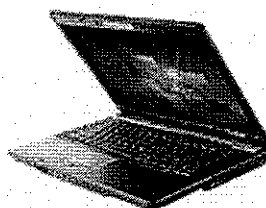


Acer Aspire 7520-5374 Notebook PC - AMD Turion™ 64 X2 Dual-Core Mobile TL-50 1.6GHz, 802.11b/g Wireless, 3GB DDR2, 250GB HDD, DVDRW, 17" WXGA+, Webcam, Windows Vista Home Premium

Buy new: **\$859.99**

In Stock

46.



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Product Details

• 1.6 GHz

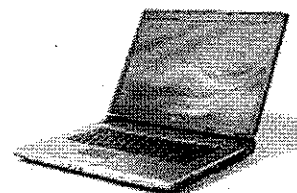
41.

No image available

Acer Aspire 5315-2077 Refurbished Notebook PC - Intel Celeron M 540 1.86GHz, 802.11b/g Wireless, 1GB DDR2 160GB HDD, CD-RW/DVD-ROM Combo, 15.4" WXGA, Windows Vista Home Basic

1 Used & new from \$399.99

44.



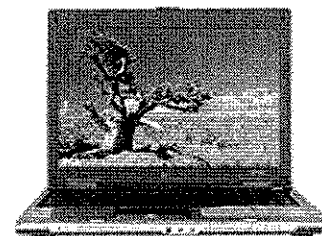
Core 2 Duo T5500, 1GB, 120GB
Buy new: ~~\$1,422.43~~ **\$842.47**

In stock. Processing takes an additional 2 to 3 days.

Product Details

• 1.66 GHz

47.



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Acer TravelMate 5520-5313 -
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Vista Business / XP Pro
downgrade - 15.4" Widescreen
TFT 1280 x 800 (WXGA)

Available at external website:
TheNerds.net for **\$674.99**

Product Details
• 1.6 GHz

Acer Aspire Celeron M 1.6GHz
512MB 80GB CDRW/DVD 14.1-
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Operating System


Any Operating System

Windows Vista Business (9)
Windows Vista Home Basic (11)
Windows Vista Home
Premium (21)
Windows Vista Ultimate (4)
Windows XP (7)

Price

Any Price

\$200-\$499 (5)
\$500-\$999 (56)
\$1000-\$1999 (18)
\$2000-\$4999 (3)

\$ to \$ 

CPU Speed

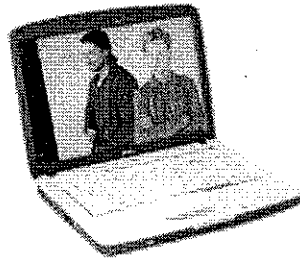
Any CPU Speed

1.5 GHz & Under (2)
1.6 to 1.9 GHz (33)
2 to 2.9 GHz (16)

Computer Platform

Any Computer Platform

1.



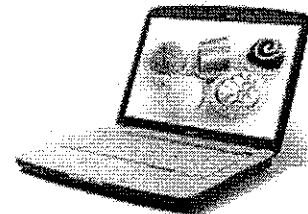
**Acer Aspire 5715-4713 Notebook
PC - Intel Pentium Dual-Core
T2370 1.73GHz, 802.11b/g
Wireless, 2GB DDR2, 160GB HDD,
Dual Layer DVD RW, 15.4" WXGA,
Webcam, Windows Vista Home
Premium**

Buy new: **\$599.99**

In Stock

★★★★★ (1)

2.



**Acer Aspire 5720-6661 15.4"
Laptop (1.5 GHz Intel Core 2 Duo
T5250 Processor, 2 GB RAM, 160
GB Hard Drive, Vista Premium)**

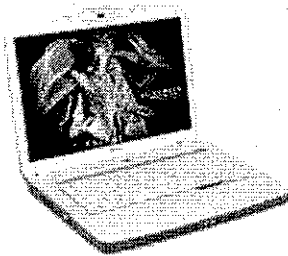
Buy new: ~~\$1,049.99~~ **\$749.99**

Get it by **Monday, April 28** if you order
in the next **20 hours** and choose one-
day shipping.

Eligible for **FREE** Super Saver Shipping.

★★★★★ (1)

4.



**Acer Aspire 5920-6954 Laptop
Computer - Intel Core 2 Duo
T5450 1.66GHz, 802.11a/b/g/n
Wireless, 2GB DDR2, 250GB HDD,
DVDRW, 15.4" WXGA, Integrated
Webcam, Windows Vista Home
Premium**

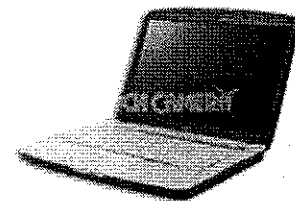
Buy new: **\$929.99**

2 Used & new from \$849.99

In Stock

★★★★★ (1)

5.



**Acer Aspire 5720-4649 15.4"
Laptop (1.46 GHz Intel Pentium
Dual Core T2310 Processor, 1 GE
RAM, 160 GB Hard Drive, Vista
Premium)**

Buy new: ~~\$699.99~~ **\$549.99**

2 Used & new from \$549.99

Get it by **Monday, April 28** if you order
in the next **20 hours** and choose one-
day shipping.

Eligible for **FREE** Super Saver Shipping.

★★★★★ (3)

PC (54)

7.

8.

Display Size

Any Display Size

- 10 to 13 in. (3)
- 14 to 15 in. (44)
- 16 to 17 in. (5)
- 20 to 29 in. (1)

Shipping Option

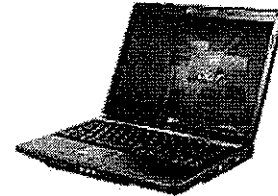
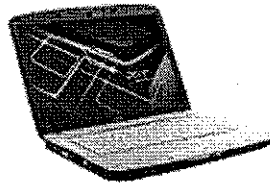
Any Shipping Option

Can be shipped within one business day from Amazon.com (2)

Related Categories

Bluetooth

New Arrivals



Acer Aspire AS5520-5908 15.4" Laptop (1.8 GHz Amd Athlon 64 X2 Dual Core TK-55 Processor, 1 GB RAM, 120 GB Hard Drive, Vista Premium)

Buy new: ~~\$643.99~~ **\$598.99**

7 Used & new from \$582.10

In Stock

Eligible for **FREE** Super Saver Shipping.

★★★★★ (3)

Product Details

- 1.8 GHz

Acer Extensa 4620-4431 14.1" Laptop (1.6 GHz Intel Pentium Dual Core T2310 Processor, 1 GB RAM, 120 GB Hard Drive, XP Pro)

Buy new: **\$664.99**

8 Used & new from \$650.08

In Stock

Eligible for **FREE** Super Saver Shipping.

Product Details

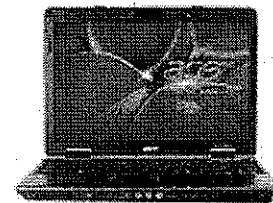
- 1.6 GHz
- 1000 MB DDR2 SDRAM



10.



11.



Acer Aspire 5050-5430 14.1" Laptop Computer (AMD Athlon 64 X2 Dual-Core TK-53, 1 GB RAM, 120 GB Hard Drive, Dual-Layer DVD-RW, WXGA, Windows Vista Home Premium)

2 Used & new from \$619.99

Acer Ferrari 5000-5832 15.4" Laptop (AMD Turion 64 X2 Mobile Processor, 2 GB RAM, 160 GB Hard Drive, DVD Drive, Vista Ultimate)

Buy new: ~~\$2,699.00~~ **\$1,599.99**

2 Used & new from \$1,599.99

In Stock

★★★★★ (3)

Product Details

- 2 GHz
- 2000 MB DDR2 SDRAM

Acer Extensa 4220-2555 14.1" Laptop (1.86 GHz Intel Celeron M 540 Processor, 1 GB RAM, 12 GB Hard Drive, XP Pro)

Buy new: ~~\$633.99~~ **\$615.07**

6 Used & new from \$587.95

In Stock

Eligible for **FREE** Super Saver Shipping

Product Details

- 1.86 GHz



13.

14.

Acer Aspire Celeron 1.73GHz 512MB 80GB CDRW/DVD 14.1" Vista

Buy new: **\$534.79**

In Stock

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Brandon Gage "brando" ☒

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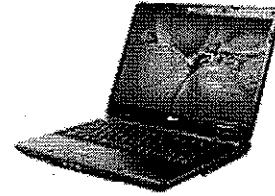


**Acer Aspire 7720-6712 Laptop
Computer - Intel Core 2 Duo
T5450 1.66GHz, 802.11a/b/g
Wireless, 2GB DDR2, 250GB
HDD, Dual Layer DVD RW, 17"
WXGA+, Windows Vista Home
Premium**

Buy new: ~~\$849.00~~ **\$849.00**

3 Used & new from \$749.00

In Stock



**Acer EX5620-6635 15.4" Laptop
(1.66 GHz Intel Core 2 Duo
T5450 Processor, 1 GB RAM, 12
GB Hard Drive, Vista Business)**

Buy new: ~~\$720.00~~ **\$702.66**

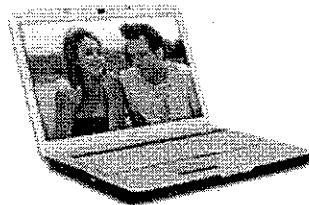
7 Used & new from \$702.66

In Stock

Product Details

• 1.66 GHz

16.



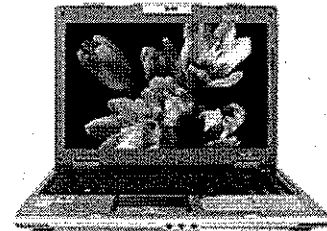
**Acer Aspire 7720-6569 Laptop
Computer - Intel Core 2 Duo
T5450 1.66GHz, 802.11a/b/g
Wireless, 2GB DDR2, 160GB
HDD, DL DVDRW, 17" WXGA+,
Integrated Webcam, Windows
Vista Home Premium**

Buy new: **\$799.99**

2 Used & new from \$699.99

In Stock

17.



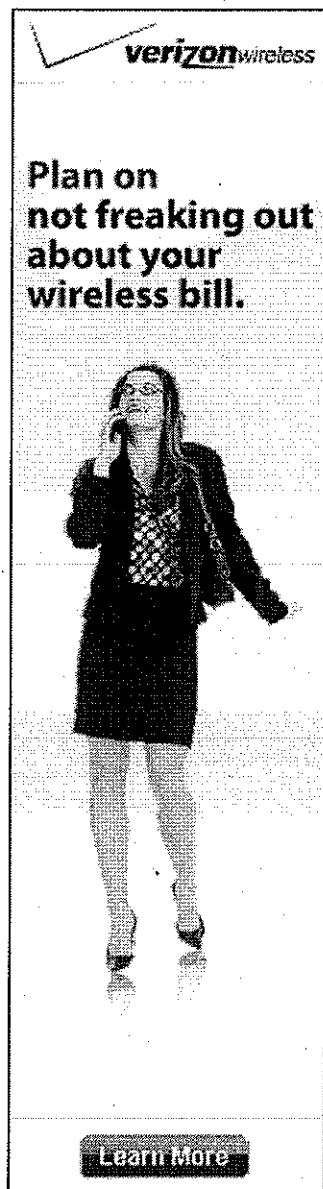
**Acer Aspire 5050-5430 14.1"
Laptop Computer (AMD Athlon
64 X2 Dual-Core TK-53, 1 GB
RAM, 120 GB Hard Drive, Dual-
Layer DVD-RW, WXGA, Window
Vista Home Premium)**

2 Used & new from \$619.99

19.

20.

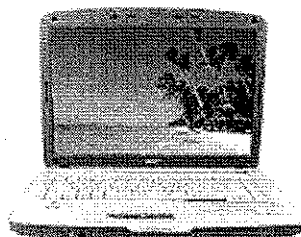
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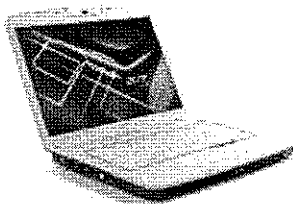
**Acer Celeron M 530 1.73GHz
1GB 80GB CDRW/DVD 15.4-Inch
Vista**

1 Used & new from \$512.79

Product Details

- 1.73 Intel Celeron
- 1024 MB DDR2 SDRAM
- 80 GB Serial ATA

22.



Core 2 Duo T7300, 2GB, 200GB

Buy new: ~~\$4,000.00~~ **\$1,699.99**

In Stock

★★★★☆ (2)

Product Details

- 2 GHz
- 2000 MB DDR2 SDRAM



Amd Turion 64 X2, 4GB, 250GB

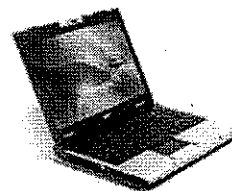
Buy new: ~~\$2,004.00~~ **\$1,869.16**

In Stock

Product Details

- 2.3 GHz

23.



**Acer Aspire 5050-4570 - Turion
64 MK-38 / 2.2 GHz - RAM 1 GB
- HDD 120 GB - DVD?RW (?R
DL) / DVD-RAM - Radeon Xpres
1100 - WLAN : 802.11b/g - Vist
Home Premium - 14.1"
Widescreen TFT 1280 x 800
(WXGA)**

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Product Details

- 2.2 GHz

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Acer

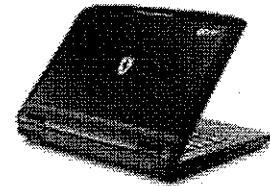
49.

50.



**Acer Aspire Dual-Core 1.73GHz
2GB 120GB DVD±RW 17-Inch
Vista**

1 Used & new from \$699.99



**Acer Ferrari 1004WTMI 12.1"
Laptop (AMD Turion™ 64 X2 TL-
56, 1 GB RAM, 160 GB Hard
Drive, DVD+/-RW/CD-RW
Drive)**

Currently unavailable

☆☆☆☆☆ (2)

Product Details

- 1.8 GHz AMD Turion 64
- 1000 MB DDR2 SDRAM
- 160 GB Serial ATA

Seller

Any Seller

- PAC Computers (23)
- Computer Geeks (20)
- Computer Brain (15)
- Amazon.com (14)
- ANTOnline (14)
- SkyBox-USA (13)
- Technology Galaxy (13)
- > [See more...](#)

Operating System

Any Operating System

- Windows Vista Business (9)
- Windows Vista Home Basic (11)
- Windows Vista Home
Premium (21)
- Windows Vista Ultimate (4)
- Windows XP (7)

52.

53.



**Acer America Corp.
LX.AWP0X.053 Turion 64 MK-36,
1GB, 120GB**

Buy new: \$1,666.34 \$900.62

In stock. Processing takes an additional
2 to 3 days.



Celeron M 430, 512MB, 80GB

Currently unavailable

Product Details

- 1.73 GHz

Price

Any Price

- \$200-\$499 (5)
- \$500-\$999 (56)
- \$1000-\$1999 (18)
- \$2000-\$4999 (3)

\$ to \$

CPU Speed

Any CPU Speed

- 1.5 GHz & Under (2)
- 1.6 to 1.9 GHz (33)
- 2 to 2.9 GHz (16)

Computer Platform

Any Computer Platform

55.

56.

PC (54)

Display Size

Any Display Size

- 10 to 13 in. (3)
- 14 to 15 in. (44)
- 16 to 17 in. (5)
- 20 to 29 in. (1)

Shipping Option

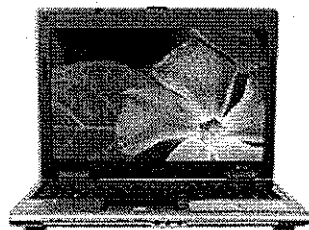
Any Shipping Option

Can be shipped within one business day from Amazon.com (2)

Related Categories

Bluetooth

New Arrivals



Acer Aspire AMD Turion 64 2.0GHz 1GB 80GB DVD±RW 14-Inch with Windows Vista Home Basic

1 Used & new from \$549.99



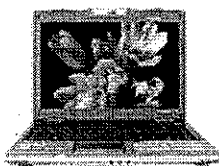
ACER COMPUTER Ferrari 3200 Notebook Computer

1 Used & new from \$1,799.99

★★★★★ (1)

Product Details

- 2.8 GHz AMD Athlon
- 512 MB PC 2700 DDR Memory
- 80 GB IDE



Acer Aspire 5050-5430 14.1" Laptop Computer (AMD Athlon 64 X2 Dual-Core TK-53, 1 GB RAM, 120 GB Hard Drive, Dual-Layer DVD-RW, WXGA, Windows Vista Home Premium)

2 Used & new from \$619.99

58.



Acer Ferrari 3200 Laptop Computer PC

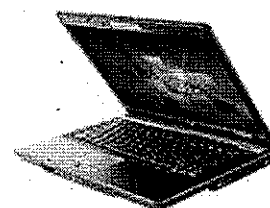
1 Used & new from \$1,799.99

★★★★★ (4)

Product Details

- 1.6 GHz

59.



Acer TravelMate 5520-5678 15.4" Laptop (1.9GHz Amd Turion 64 X 2 Dual Core TL-58 Processor, 1 GB RAM, 120 GB Hard Drive, Vista Business)

Buy new: \$734.99 \$731.98

6 Used & new from \$702.75

In Stock

Eligible for **FREE** Super Saver Shipping

Product Details

- 1.9 GHz



Acer Aspire Celeron 1.73GHz 512MB 80GB CDRW/DVD 14.1" Vista

Buy new: \$534.79

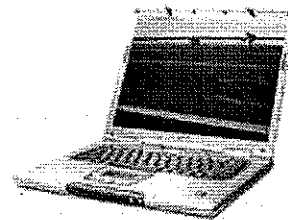
In Stock

61.



Acer Aspire 3100-1405 15.4" Laptop (AMD Sempron

62.



Amd ATHLON64

Listmania!



My favourite Laptop: A list
by S.R - Electronics
Enthusiast ☒



Great Gadgets: A list by
Rat Singanl "R Mann" ☒

► Create a Listmania! list

Search Listmania!



Processor 3500+, 512 MB RAM, 80 GB Hard Drive, Vista Basic)

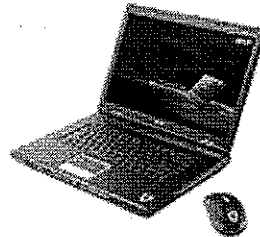
Currently unavailable

★★★★☆ (2)

Product Details

- 1.8 GHz AMD Sempron
- 512 MB DDR2 SDRAM
- 80 GB Serial ATA

64.



3000+, 512MB, 80GB

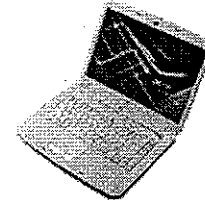
2 Used & new from \$1,599.99

★★★★☆ (2)

Product Details

- 2.0 GHz AMD Mobile Athlon 64
- 512 MB PC 2700 DDR Memory
- 80 GB IDE

65.



Acer Ferrari 4005WLMi 15.4" Laptop (AMD Turion 64 Mobile Technology ML-37, 1 GB RAM, 100 GB Hard Drive, DVD Super- Multi Dbl Layer Drive)

1 Used & new from \$1,799.99

★★★★☆ (10)

Product Details

- 2 GHz

67.



Acer Aspire 5720-4230 15.4" Laptop (1.6 GHz Intel Pentium Dual Core T2330 Processor, 1 GB RAM, 120 GB Hard Drive, Vista Premium)

Buy new: **\$666.99**

7 Used & new from \$650.10

In Stock

Eligible for **FREE** Super Saver Shipping

Product Details

- 1.6 GHz

68.



Core Duo T1350, 512MB, 80GB

Currently unavailable

Product Details

- 1.86 GHz

70.

Acer Ferrari 4005WLMi - Turion 64 ML-37 / 2 GHz - RAM 1 GB - HDD 100 GB - DVD?RW / DVD- RAM - Mobility Radeon X700 - Gigabit Ethernet - WLAN : 802.11b/g, Bluetooth - Win XP Pro - 15.4" Widescreen TFT 1680 x 1050 (WSXGA+)

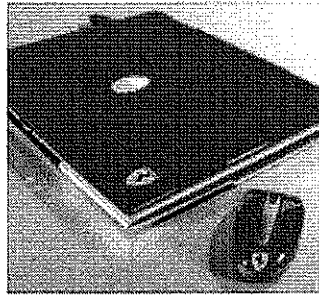
1 Used & new from \$1,799.99

Product Details

- 2 GHz

71.

ADVERTISEMENT



No image
available

ACER Ferrari 3400LMI notebook
Mobile Athlon 64 AMD3000+
15.0" SXGA+ 512MB DDR333
80GB 4200rpm DVD Super Multi
ATI Mobility RADEON 9700

1 Used & new from \$1,799.99

★★★★★ (2)

Product Details

- 2.0 Athlon 64
- 512.0 DDR2 SDRAM
- 80.0 ATA133

Acer Ferrari 3400LMI - Mobile
Athlon 64 3000+ / 2 GHz - RAM
512 MB - HDD 80 GB - DVD?
RW / DVD-RAM - Mobility
Radeon 9700 - Gigabit Ethernet
- WLAN : 802.11b/g, Bluetooth
Win XP Home - 15" TFT 1400 x
1050 (SXGA+)

1 Used & new from \$1,799.99

Product Details

- 2 GHz

Showing 49 - 72 of 84 Results

« Previous | Page: 1 2 3 4 | Next

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EXHIBIT H

**TO THE DECLARATION OF JOHN L. COOPER IN
SUPPORT OF MOTION TO DISMISS AND TO
TRANSFER**

Gateway recommends Windows Vista® Home Premium.

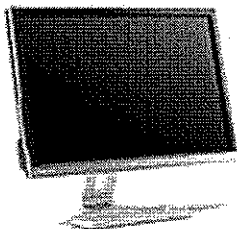
Order by Phone: 800



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Retail Products Notebooks Desktops Displays Accessories



Gateway® HD2200 22" Widescreen HD LCD Display

The Hub of Your Digital Entertainment Gateway's HD2200 features exceptional technology with widescreen viewing and advanced features to improve productivity and



1 - 3 of 3 25 Rows Per Page

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In Stock

Address

Yes

Longview, TX

[See



Call

Longview, TX

[See



Call

Longview, TX

[See



1 - 3 of 3 25 Rows Per Page

While every reasonable attempt has been made to check on the validity of the availability, location, product and pricing info provided, we cannot guarantee that the information provided is without error. Stock status reported is an accurate representation of dealer information as of the date and time shown. "Yes" stock status does not guarantee availability, please check directly with the dealer listed. Company logos, product and service names may be trademarks or service marks of the respective companies.

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EXHIBIT I

**TO THE DECLARATION OF JOHN L. COOPER IN
SUPPORT OF MOTION TO DISMISS AND TO
TRANSFER**

10-K 1 d10k.htm FORM 10-K

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UNITED STATES SECURITIES AND EXCHANGE COMMISSION

Washington, D.C. 20549

FORM 10-K

(Mark One)

☒ ANNUAL REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES
EXCHANGE ACT OF 1934

For the fiscal year ended December 31, 2006

OR

☐ TRANSITION REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES
EXCHANGE ACT OF 1934

For the transition period from _____ to _____

Commission file number 1-14500

GATEWAY, INC.

Incorporated in Delaware

I.R.S. Employer Number
42-1249184

7565 Irvine Center Drive, Irvine, CA 92618-2930

Telephone number: (949) 471-7000

Securities registered pursuant to Section 12(b) of the Act:

Title of each class	Name of each exchange on which registered
Common Stock, par value \$.01 per share	New York Stock Exchange
Preferred Share Purchase Rights	New York Stock Exchange

Securities registered pursuant to Section 12(g) of the Act: None

Indicate by check mark if the registrant is a well-known seasoned issuer, as defined in Rule 405 of the Securities Act. Yes ☒ No ☐

Indicate by check mark if the registrant is not required to file reports pursuant to Section 13 or Section 15(d) of the Act. Yes ☐ No ☒

Indicate by check mark whether the registrant: (1) has filed all reports required to be filed by Section 13 or 15(d) of the Securities Exchange Act of 1934 during the preceding 12 months (or such shorter period that the registrant was required to file such reports); and (2) has been subject to such filing requirements for the past 90 days. Yes ☒ No ☐

Indicate by check mark if disclosure of delinquent filers pursuant to Item 405 of Regulation S-K is not contained herein, and will not be contained, to the best of registrant's knowledge, in definitive proxy or information statements incorporated by reference in Part III of this Form 10-K or any amendment to this Form 10-K. ☐

Indicate by check mark if the registrant is a large accelerated filer, an accelerated filer, or a non-accelerated filer. See definition of "accelerated filer and large accelerated filer" in Rule 12b(2) of the Exchange Act. (Check one).

Large accelerated filer ☒ Accelerated filer ☐ Non-accelerated filer ☐

Indicate by check mark whether the registrant is a shell company (as defined in Rule 12b-2 of the Exchange Act). Yes ☐ No ☒

The aggregate market value of the voting stock held by non-affiliates of the registrant on June 30, 2006, the last business

day of the registrant's most recently completed second fiscal quarter (based on the last sale price on the New York Stock Exchange as of such date) was approximately \$705,003,902.

As of February 20, 2007 there were 371,517,940 shares of Common Stock outstanding and no shares of Class A Common Stock outstanding.

DOCUMENTS INCORPORATED BY REFERENCE

Portions of Gateway's Definitive Proxy Statement to be filed in connection with our 2007 Annual Meeting of Stockholders subsequent to the date hereof are incorporated by reference in Part III of this Form 10-K. Such Definitive Proxy Statement will be filed with the Securities and Exchange Commission no later than 120 days after the Registrant's year end of December 31, 2006.

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GATEWAY, INC.
FORM 10-K
For the Fiscal Year Ended December 31, 2006

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Forward-Looking Statements—This Annual Report on Form 10-K, including “Management’s Discussion and Analysis of Financial Condition and Results of Operations” in Item 7, contains forward-looking statements based on Gateway’s current expectations that are subject to various risks and uncertainties, as well as assumptions that, if they do not materialize or prove incorrect, could cause our future results to differ materially from those expressed or implied by such forward-looking statements. All statements other than statements of historical fact are statements that are or could be deemed forward-looking statements, including without limitation any statements relating to future results of operations, plans, outlook or strategies, any statements relating to execution of restructuring plans or regarding pending claims or disputes and any statements relating to future economic or industry conditions. Factors that might cause such differences include, but are not limited to, those discussed in “Risk Factors” in Item 1A, or that are otherwise described from time to time in our reports filed with the Securities and Exchange Commission after this Annual Report. Gateway assumes no obligation to update any forward-looking statements to reflect events that occur or circumstances that may arise after the date as of which they are made.

Throughout this Annual Report we refer to Gateway, Inc. and its consolidated subsidiaries as “Gateway,” “the company,” “we,” “us,” and “our.”

This Annual Report contains the following trademarks and service marks of Gateway which are registered: Gateway, eMachines, and the “Black-and-White Spot” Design. These and any other product or brand names of Gateway or of any other company contained herein are trademarks or registered trademarks of their respective owners.

PART I

Item 1. *Business*

General

Gateway directly and indirectly sells its desktop and notebook computers and servers (“PCs”) and PC-related products and services that are enabled by or connect with PCs to third-party retailers, consumers, businesses, government agencies and educational institutions. Gateway offers its PCs under two brand names, Gateway and eMachines, and positions each of its products on the basis of relative value for money with eMachines systems being offered at lower price points and Gateway systems being offered with higher-end chipsets and richer features at attractive prices that represent value. PC-related products and services (“Non-PC”) consist of all products and services other than the PC, such as stand-alone displays, peripherals, software, accessories, extended warranty services, training, Internet access, enterprise system and networking products and services. Gateway was the third largest PC company in the U.S. during calendar 2006 and among the top 10 worldwide, with an estimated U.S. market share of approximately 6.7% based on units shipped, according to the most recent data from International Data Corporation.

Gateway’s strategy is to profitably grow its core PC business by driving to be a low cost provider while improving operational execution and overall efficiency. Gateway is focused on growing its consumer business through both its Direct and Retail channels via product innovation, retail relationships, an enhanced web presence and leveraging its investments in the Professional business for profitable growth in targeted markets.

Business Segments

Gateway has three major business segments: Retail, Professional, and Direct. Further information on Gateway’s business segments can be found in Item 7 “Management’s Discussion and Analysis of Financial Condition and Results of Operations” and Note 11 to the Consolidated Financial Statements.

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Retail (including International)

The Retail segment is Gateway's largest segment. Gateway and eMachines products are sold in more than 7,000 retail locations in the U.S. and Canada. Gateway sells products directly to consumer electronics stores, computer superstores, and other major retailers such as Best Buy, Circuit City, CompUSA, Costco, Office Depot, Micro Center, Wal-Mart and many others, as well as selling select Gateway-branded products through television shopping retailers. Sales to Best Buy represented 39% of net sales in 2006 and 34% of net sales in 2005. The company's eMachines-branded products are sold exclusively through the retail channel. Gateway participates in cooperative advertising and marketing programs with key retail customers, for which it receives marketing development funds from key suppliers to partially pay for advertising that features their brands.

Prior to the acquisition of eMachines in 2004, Gateway's international sales were limited to Canada and Mexico while eMachines sold its products internationally in Japan and the United Kingdom. After the eMachines acquisition, Gateway took advantage of each company's distribution channels and implemented common supply chain management techniques and service infrastructures to expand distribution within Canada, Japan, Mexico and the United Kingdom. Gateway and eMachines products are sold in more than 3,400 retail locations internationally.

Substantially all international sales are through third-party retailers and distributors. Gateway continues to evaluate opportunities to develop and grow the international business, currently focusing on Western Europe and Asia. Approximately 8% of net sales in 2006 and approximately 7% of net sales in 2005 came from sales to customers outside the U.S. and Canada.

Professional

The Professional segment's sales and marketing activities focus on core market customers: small-to-medium businesses, educational institutions (K-12 and higher education) and government agencies (federal, state and local). Sales are conducted through telephone-based and field sales teams, complemented by local, regional and national value-added resellers. The company also sells its products to its Professional segment customers through customized websites.

Gateway's custom integration solutions program is designed to accommodate the needs of large professional customers who require specialized hardware, software and services that are not available as part of standard offerings. The company's custom integration solutions program accelerates technology deployment for clients through integration of unique hardware and software and development of customized services to meet the individual requirements of professional customers.

Direct

The Direct segment is focused on selling individually-customized, Gateway-branded products and services as well as complementary third-party products and services directly to U.S. consumers and small business customers. The company markets its Direct products through television and print advertising, e-mail, direct mail, Internet advertising, and its website at www.gateway.com.

Gateway sells its Direct products and services in the U.S. primarily through its www.gateway.com website and its U.S.-based call centers (1-800-GATEWAY).

PC Products, Servers and Storage

Gateway offers its customers a broad line of Gateway and eMachines-branded PCs and Gateway-branded servers. The company markets its PCs with recommended configurations, but its customers can also

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configure-to-order some Gateway-branded PCs with a choice of microprocessors, memory, storage and optical drives, as well as other options. The following are the key products within this class:

Desktop PCs. Gateway offers a series of desktop PC products, developed to serve targeted customer segments. The company offers a range of standard models for consumers under the eMachines and Gateway brands and for professional customers under the Gateway brand, with each series having a number of recommended configurations with varying levels of technology and features. Customers can purchase certain models of Gateway-branded PCs that they customize for their particular needs. Desktops represented approximately 47% of net sales in 2006 and approximately 49% of net sales in 2005.

Notebook PCs. Gateway offers a series of notebook PC products to provide mobile computing capabilities for both consumer and professional customers. The systems are generally available with docking stations, wireless enablement and various multimedia applications. As with desktops, notebooks have a range of standard model series, with each series having a number of recommended configurations. The systems range from convertible tablets to high-performance desktop replacement class notebooks. Notebook PCs represented approximately 36% of net sales in 2006 and approximately 31% of net sales in 2005.

Servers and Storage. Gateway also offers Gateway-branded servers and storage products for professional and small business customers. Every Gateway server has an adaptable design and can be custom built with a variety of options to fit the customer's needs. Gateway servers can be ordered in tower-based or rack-mounted configurations, with Microsoft Windows® operating software. Servers and storage products represented approximately 1% of net sales in 2006 and approximately 2% of net sales in 2005.

Non-PC Products and Services

Non-PC products and services consist of all products and services other than the PC, such as stand-alone displays, peripherals, software, accessories, extended warranty services, training, Internet access, and enterprise system and networking products and services. Non-PC products and services represented approximately 16% of net sales in 2006 and approximately 18% of net sales in 2005.

Stand-Alone Displays, Peripherals, Software and Other PC-Related Products. Gateway markets stand-alone displays, printers, projectors, computer memory, scanners, PC accessories, CD and DVD burners, storage devices, surge protectors, and other PC accessories that are manufactured by leading companies in their respective markets. Gateway offers a complete line of thin film transistor and cathode ray tube displays. These displays are sold with desktop PCs through Gateway's channels and are also available for stand-alone purchase. The company offers a limited number of Non-PC products under the Gateway brand. In addition, we market a broad range of third-party software offerings, from entertainment and productivity applications for the consumer market to vertical applications for various segments of the commercial and institutional markets.

Service Programs. Gateway offers value-added, fee-based service and support consisting of Internet access, web portal, security, extended service plans, including extended technical support and warranty services, accidental damage programs, and learning and tutorial services sold mostly on behalf of third party service providers.

In addition, Gateway's Professional segment offers value-added service and support offerings that are designed to satisfy the needs of businesses throughout the technology lifecycle. Gateway utilizes a network of third-party providers who work with our professional sales force to deliver local consultation and integration services to business, education and government customers in essentially all the top markets across the United States. In this segment, Gateway offers:

- Technology planning services, such as on-site consultation and network design services;
- Implementation services, such as custom installation and imaging, asset tagging, and hardware and network installation;
- Productivity services, such as customized learning solutions, network and application support, and custom helpdesk solutions;

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- Maintenance services, such as on-site and product exchange services; and
- End of life services, such as data migration, deinstallation and asset recovery services.

Multi-Channel Delivery. Gateway delivers customer service and support at the customer's location, at third-party locations and via telephone and the web. Gateway believes the availability of services through multiple channels benefits customers by providing them with a range of service options. Most support services are provided by third-party vendors, but the company also provides technical telephone support services through its U.S. based "Best Practices Center". This Center is made up of Gateway employees who develop problem resolution procedures and technical solutions for Gateway products which are then distributed to the third-party service providers.

Financing Programs. Gateway has arrangements with third-party financing institutions that provide financing to Direct and Professional customers for the purchase or lease of the company's products.

Cooperative Product Development

The PC industry is characterized by rapid technological advances. Gateway's ability to compete successfully is heavily dependent upon the ability to ensure a continuing and timely flow of competitive products and technology to the marketplace. The company's focus is primarily on coordinating and leveraging the development activities of a number of key technology partners, original design manufacturers and product or component providers. Gateway's product development efforts are focused on designing and developing competitively priced PC systems and Non-PC products that adhere to industry standards and incorporate the technologies and features that Gateway believes are most desired by its customers.

Gateway relies on cooperative relationships with a range of suppliers and other technology developers for engineering, product development and production support in the fulfillment of its desktop and notebook computer and server product lines. Working with these companies, Gateway's engineers manage quality, integrate technologies and design product and system architecture. Gateway believes that these relationships, together with market information obtained from its customer relationships, allow it to rapidly introduce and deliver appealing new products, software and services to the marketplace.

Manufacturing

Gateway's product needs are fulfilled through original design manufacturing and distribution relationships in Asia, Europe, Mexico and the United States to meet the needs of key market segments. The company's manufacturing and distribution supply base operates under Gateway work instructions to assure the functional specifications and quality. In addition, engineering and quality assurance teams help ensure that products meet Gateway specifications and applicable regulatory requirements.

To better serve its Professional and Direct customers, Gateway opened a dedicated U.S. final assembly facility in 2006 at which Gateway assembles configure-to-order desktops, notebooks and servers according to customer specifications. Gateway also provides custom imaging services and government compliance certification.

Patents, Trademarks and Licenses

Gateway, including AD Technologies LLC (formerly known as Amiga Development LLC), has over 400 U.S. utility patents and a number of related foreign patents, and Gateway has a significant number of pending U.S. and foreign patent applications. Gateway has a majority equity interest in AD Technologies LLC, a holding company for intellectual property, which is controlled by Gateway's founder, Ted Waitt. A majority of the patents in the portfolio were issued in the last five years. The company's patent strategy focuses on building a

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broad portfolio of patents in the areas of computer related and information processing technologies, consumer electronics and manufacturing processes for defensive purposes. Generally, Gateway's products incorporate industry standard technology rather than proprietary technology it develops.

Gateway owns and uses a number of trademarks, brands and service marks on or in connection with its products and services, including Gateway, eMachines and the "Black-and-White Spot" design, among others. Many of these trademarks are registered in the United States and other countries, and numerous trademark applications are pending in the United States and other countries. The company believes these trademarks have strong brand name recognition in the United States marketplace and in many countries throughout the world.

Gateway also licenses technologies and software from third parties for integration into its products. Some of these technologies are industry standard technologies which are licensed by many of its competitors. In addition, certain companies are increasingly engaging in the business of acquiring or developing patents to assert offensively against companies such as Gateway, and some of its direct and indirect competitors seek to license their technology. As a result, Gateway may incur license costs that its competitors do not incur. Gateway generally does not own the software used on its PCs and has entered into software licensing arrangements with a number of software developers, including Microsoft Corporation for Windows® and Microsoft Office software products, among others.

Competition

The PC industry is characterized by a handful of large competitors, numerous smaller competitors, aggressive pricing, short product life cycles, and price sensitivity by customers. The level of pricing aggressiveness continues to be intense, particularly in the low-price end of the market. In addition, some of Gateway's current and potential partners, including original design manufacturers, design, manufacture and often market their products under their own or third-party brand names. Many of Gateway's competitors are larger and better funded than Gateway.

Gateway's primary competitors in the PC area are Dell Inc., Hewlett-Packard Company, Apple Inc., Lenovo Group Limited, Sony Corporation, Acer Inc. and Toshiba Corporation. In particular regions and outside of the U.S., Gateway faces additional competition from companies such as Fujitsu Limited and Packard Bell. Gateway also faces competition from generically-branded or "white box" manufacturers.

Gateway competes primarily on the basis of customer satisfaction, price, product value, technology, product offerings with innovative performance features, quality, reliability, brand recognition, customer service and support and by maintaining strategic supplier relationships that enable it to bring products to market quickly.

Historically, Gateway and many of its competitors have regularly lowered prices. Gateway expects these competitive pressures to continue in 2007 and that average sales prices for PCs and Non-PC products will continue to decline.

Environment

Certain of Gateway's operations involve the use of substances regulated under various federal, state and international laws governing the environment, including those governing the discharge of pollutants into the soil, air and water, the management and disposal of hazardous substances and wastes, and the cleanup of contaminated sites. Certain of Gateway's products are subject to various federal, state and international laws governing chemical substances in products, including those regulating the manufacture and distribution of chemical substances and those restricting the presence of certain substances in electronics products. Gateway also faces increasing complexity in its product design, procurement and operations as it adjusts to new and upcoming requirements relating to the composition of its products, including restrictions on the use of lead and other substances in electronics that apply to products sold in the European Union after July 1, 2006. In addition,

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Gateway is subject to costs and liabilities in connection with product take-back legislation in certain jurisdictions that impose financial responsibility on producers of electrical goods for specified collection, recycling, treatment and disposal of covered products. Gateway currently has an incentive program to encourage its PC customers to recycle or donate their old PCs and displays, regardless of brand, and Gateway is working with its original design manufacturers and suppliers to reduce the use of hazardous substances in its products. Environmental costs are presently not material to Gateway's operations or financial position; however, such costs may become material in the future as compliance obligations continue to increase.

Employees

As of December 31, 2006, Gateway had approximately 1,700 employees, a reduction from approximately 1,800 employees as of December 31, 2005 and from 1,900 employees as of December 31, 2004, substantially all of whom are located in the United States. Gateway believes it has generally good relationships with its employees.

Backlog

The backlog of unfilled orders was approximately \$98 million at December 31, 2006 and approximately \$73 million at December 31, 2005. Gateway does not believe that backlog is a meaningful indicator of sales that can be expected for any period. There can be no assurance that the backlog at any point in time will translate into sales in any subsequent period, particularly in light of the company's policy, which allows customers to cancel or reschedule orders.

Seasonality

Historically, revenues in the Retail segment are higher during the second half of the year. Gateway's Professional segment revenues are traditionally stronger in the second and third quarters. However, these patterns are subject to overall general economic market conditions, large bulk buys and technology transitions.

Available Information

You can access additional information about Gateway and its products and services at www.gateway.com and www.emachines.com. You can also access Gateway's Annual Reports on Form 10-K, Quarterly Reports on Form 10-Q, Current Reports on Form 8-K, and any amendments to these reports, free of charge, on Gateway's website at www.gateway.com, after the company files the reports with or furnishes them to the Securities and Exchange Commission. Gateway will also provide these reports in printed form to any stockholder who requests them from Gateway. The information on the website is not incorporated into this Annual Report.

The SEC also maintains an Internet website that contains reports, proxy and information statements and other information regarding issuers, such as Gateway, that file electronically with the SEC. The SEC's Internet website is located at www.sec.gov.

Corporate Governance

Gateway's Board of Directors is elected by Gateway's stockholders and is responsible for directing the management of business and affairs of Gateway. Gateway's Chief Executive Officer and senior management run Gateway's day-to-day business operations. The Board has adopted formal Corporate Governance Guidelines which are available at www.gateway.com and will be provided in printed form to any stockholder who requests a copy from Gateway. The guidelines provide that the principal responsibilities of the Board, in addition to its general oversight responsibilities, include the: (a) selection, evaluation and compensation of the Chief Executive Officer and oversight of the selection and compensation of Gateway's senior executive management; (b) oversight of succession plans for the Chief Executive Officer and key executive positions; (c) review and

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evaluation and, as appropriate, approval of Gateway's financial and business performance, operations, key objectives, strategies, plans and actions; and (d) review of the processes in place to ensure the integrity of Gateway's financial, accounting and control systems and the accounting principles and practices used to prepare the financial statements.

The current Board consists of nine directors, eight of whom are independent directors under the rules of the New York Stock Exchange. The other director, Ed Coleman, is Gateway's Chief Executive Officer. In addition, as required by New York Stock Exchange rules, the Board of Directors has affirmatively determined that each independent director has no material relationship with Gateway (directly or as a partner, stockholder, or officer of any organization that has a relationship with Gateway). The Board meets in regularly scheduled meetings as well as in special meetings. All independent directors meet without management present during each regularly scheduled Board meeting, with a designated independent Board member chairing that segment of the meeting.

The Board has delegated a number of responsibilities to various committees of the Board. At the present time, the Board Committees are the Audit, Compensation, and Corporate Governance and Nominating Committees. The members of each committee are appointed by the Board. Each committee consists entirely of independent directors. Each committee meets on a regularly scheduled basis and operates under a written charter approved by the Board, all of which are available at www.gateway.com and will be provided in printed form to any stockholder who requests a copy from Gateway.

The Audit Committee represents the Board in its general oversight of Gateway's financial reporting, internal controls and audit functions. The Audit Committee is also directly responsible for the appointment, compensation and oversight of the work of Gateway's independent registered public accounting firm. For both 2005 and 2006, Deloitte & Touche LLP was appointed the independent registered public accounting firm of Gateway. This appointment was also ratified by Gateway's stockholders. The Audit Committee has again appointed Deloitte & Touche LLP as Gateway's independent registered public accounting firm for 2007, subject to stockholder approval. The Audit Committee also pre-approves any non-audit services by the independent registered public accounting firm. The Audit Committee meets regularly in separate sessions with senior management, internal audit staff and Gateway's independent registered public accounting firm.

The Compensation Committee reviews and approves salaries, bonuses and other compensation for the Chief Executive Officer and other senior executive management. In addition, the Compensation Committee administers the *2000 Equity Incentive Plan*, including reviewing and granting equity awards to officers and other employees.

The Corporate Governance and Nominating Committee reviews and reports to the Board concerning corporate governance matters, conducts an annual evaluation of the performance of the Board, and reviews and reassesses the adequacy of the Corporate Governance Guidelines. In addition, the Corporate Governance and Nominating Committee recommends to the Board the size and composition of the Board, establishes procedures for consideration of candidates for the Board and recommends specific candidates for election to the Board.

As part of Gateway's corporate governance practices, the company maintains a Code of Ethics that is applicable to all employees, including the Chief Executive Officer, Chief Financial Officer, Principal Accounting Officer and Controller, and the Board of Directors. Gateway provides ethics training to new employees when they are hired and to existing employees periodically. An Ethics Council, consisting of senior executive officers appointed by the Board, reviews reported ethical issues, including complaints through Gateway's confidential ethics hotline. The Ethics Council advises the Audit Committee with respect to ethical matters. The Audit Committee must evaluate actual or potential waivers of conflicts-of-interest for all executive officers and directors and make recommendations to the Board concerning any action to be taken. The Board conducts an annual review of the Code of Ethics. Gateway's Code of Ethics is available at www.gateway.com and will be provided in printed form to any stockholder who requests it from Gateway.

In addition, stock ownership guidelines have been established for directors and senior executive officers to better ensure that they maintain an equity stake in Gateway, and by doing so appropriately link their interests

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with those of the other stockholders. The Board guidelines provide that directors should hold Gateway common stock equal to the lesser of (a) the number of shares having a value of three times the Board member's annual cash retainer, and (b) the number of unrestricted shares granted to the director during the preceding six years. The executive officer guidelines provide that, absent unusual personal circumstances, Gateway's Chief Executive Officer and each Senior Vice President should retain 30 percent of all after tax profit shares from stock options exercised and stock grants (restricted or otherwise) for at least 3 years (from exercise or vesting date) unless the value of his or her ownership in Gateway securities exceeds five times the base salary for the Chief Executive Officer or two and a half times the base salary for Senior Vice Presidents.

Gateway continues to evaluate its corporate governance practices in light of best practices and changing regulatory requirements and anticipates additional changes as necessary or appropriate. In 2006, Gateway filed with the New York Stock Exchange an executed certification from its then interim Chief Executive Officer stating that he was not aware of any violation by Gateway of the New York Stock Exchange's corporate governance rules with respect to the 2005 fiscal year.

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Item 1A. Risk Factors

In addition to other information contained in this Annual Report, the following factors could affect Gateway's future business, results of operations, cash flows or financial position, and could cause future results to differ materially from those expressed in any of the forward-looking statements contained in this Annual Report.

The PC industry is extremely competitive and pricing pressures have reduced Gateway's gross profits and challenge its ability to maintain profitability.

Consolidation in the PC industry has resulted in larger and stronger competitors in many of Gateway's markets and it continues to experience increased competition in certain of its business segments. Gateway competes primarily on the basis of customer satisfaction, price, product value, technology, product offerings with innovative performance features, quality, reliability, brand recognition, customer service and support, and by maintaining strategic supplier relationships that enable it to bring products to market quickly. Gateway's management expects these competitive pressures to continue into the foreseeable future. Gateway's management also expects that average sales prices of its PCs will continue to decline, although this may be partially offset by an increased product mix of relatively higher priced notebook PCs, Gateway branded PCs in Retail and liquid crystal displays. If Gateway continues to reduce PC prices in response to competition, Gateway may be unable to maintain or improve gross profits through cost reductions or offsetting sales of higher margin Non-PC products. Its overall gross profit as a percentage of sales has declined due to its shift in overall distribution to third party retail and competitive pressures. To the extent Gateway is unable to maintain or grow its revenues and market share and maintain or improve its gross profits, its business prospects and financial condition would be adversely affected.

Reliance upon third-party patents and intellectual property licensing could limit Gateway's ability to innovate and exposes it to actual and potential litigation, which could adversely impact operating results.

There is no assurance that Gateway will continue to have access to existing or new third-party technology for use in its products. While it may be necessary in the future to seek or renew licenses relating to various aspects of its products and business methods, Gateway's management believes that based upon past experience and industry practice, such licenses generally can be obtained on commercially reasonable terms. However, there is no assurance that the necessary licenses would be available on acceptable terms. If Gateway or its suppliers are unable to obtain such licenses, Gateway may be forced to market products without certain desirable technological features. Gateway could also incur substantial costs to redesign its products around other parties' protected technology.

Because of technological changes in the PC industry and the convergence of PCs with Non-PC products, current extensive patent coverage, and the rapid rate of issuance of new patents, it is possible certain components of Gateway's products and business methods may unknowingly infringe upon existing patents of others. For example, Gateway is a party to various lawsuits and claims, including assertions of patent infringements and intellectual property-related administrative proceedings that arise in connection with its business. Gateway cannot predict the outcome of these matters with certainty. Some of these lawsuits allege substantial damages and also seek injunctive relief to stop it from selling products alleged to infringe patents of others. If such relief was granted or substantial damages were incurred, Gateway's business and results of operations would be materially adversely affected. In addition, responding to such claims, regardless of their merit, is time consuming, results in significant expenses, and diverts the attention of management and technical personnel.

Gateway attempts to transfer the risk of inadvertent patent infringement to its original design manufacturers and suppliers via contract. Gateway is not always successful in contractually transferring such risk to its original design manufacturers and suppliers, and even when it does so it may be unable to enforce their obligations or they may be unable to adequately defend any patent infringement claims against its PCs and Gateway-branded Non-PC products. If Gateway is unable to impose upon its original design manufacturers and suppliers the costs of patent infringement claims, its future operating results and financial condition could be materially adversely affected.

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Because one customer accounts for a substantial portion of Gateway's revenues, the loss of this customer would cause a significant decline in its revenues.

A single customer, Best Buy, accounted for approximately 39% of total revenues for 2006, up from 34% of total revenues for 2005, and is expected to continue to be a significant customer in the future. Although Gateway works to expand and diversify its customer base, reductions or terminations of product purchases by, or pricing pressures from, this customer or other major third-party retailers without an offsetting increase in new sales to other customers, would result in a substantial decline in revenue and operating results.

Failure to develop and maintain relationships with several key third-party retailers could adversely affect revenues.

Gateway's products are sold primarily through direct channels and third-party retailers. Third-party retail sales have expanded significantly since early 2004. Gateway's management expects a substantial portion of its future sales will be to a small number of key third-party retailers. Additionally, third-party retailer orders may vary considerably from quarter to quarter. If the financial condition of these retailers weakens or if they were to cease or significantly reduce the distribution of Gateway's products, Gateway's business and financial results could be adversely affected. If significant variability is experienced, Gateway's business and financial results for a particular quarter could be adversely affected. In addition, failure to foster and maintain strategic relationships with these retailers could have a significant adverse impact on Gateway's revenues and operating results.

If Gateway fails to attract new customers, retain its existing customers and/or replace revenues associated with its higher-margin service revenues, its operating results will be adversely impacted.

The success of Gateway's business depends on increasing the overall number of customer transactions in a cost-effective manner. To do this, Gateway must attract new and repeat customers through its various marketing channels, including its website, its telephone call centers, its professional sales force, and its third-party retail partners, and then convert these interactions into sales transactions. Gateway's reduced marketing expenditures have contributed in part to reduced demand within its Direct and Professional segments and Gateway's ability to successfully bid on future public sector business could be negatively impacted if Gateway fails to perform under any of its existing public sector contracts. Furthermore, some of its third-party retail partners sell or may sell private label PCs at competitive prices and these sales have the potential to adversely affect Gateway's market share. In addition, a portion of Gateway's revenue and profit is derived from higher-margin Internet access services and extended warranties sold in prior periods and recognized over time under its revenue recognition policy, which Gateway expect to decline in the future. If Gateway does not achieve increased transaction volume, or replace its higher margin service revenues with alternative sources of profit margin, its ability to grow and maintain profitability will be adversely impacted.

Information technology systems integration issues could disrupt Gateway's internal operations, which could have significant adverse effects on its profitability and/or may have a material effect on its internal controls over financial reporting.

Gateway is implementing a new enterprise resource planning ("ERP") system, as well as order capture and customer service applications, and continues to develop and modify certain of its other systems. Gateway has experienced development and implementation delays with certain projects, and may experience interruptions in availability of portions of its information technology infrastructure, additional delays in development and implementation, or unanticipated system errors. Gateway may not be successful in implementing these new systems, and transitioning data and other aspects of the process could be expensive, time consuming and disruptive. Any disruptions that may occur in the implementation of these new systems or any future systems could adversely affect Gateway's ability to report in an accurate and timely manner the results of its financial operations and otherwise efficiently operate its business, which could have significant adverse effects on its profitability.

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Gateway started implementing a significant portion of the ERP during December of 2006 which will impact a number of its internal and reporting controls. While Gateway believes it has adequately planned for the implementation and review of all noted controls, no assurance can be made that it will meet all of its financial control requirements. Gateway is reporting a material weakness in its design of internal controls in this reporting period related to its receiving and selling of components with its original design manufacturers (see Item 9A).

Gateway is dependent on manufacturing and services provided by a limited number of third parties and failure to properly manage these relationships could significantly impact its results of operations.

Gateway is dependent upon third-party providers of manufacturing and support services. Gateway currently outsources a substantial portion of its manufacturing operations, a significant portion of its service and support functions, and some administrative and operational services to third-party providers under contract. Although Gateway has partnered with certain vendors, Gateway has no assurance that business interruptions will not occur or that these third parties will meet the needs of its business. If Gateway is unable to properly manage its relationships with these third-party providers or accurately forecast its demand requirements for them, its revenues and gross profits may be adversely affected. Similarly, if its third-party providers do not comply with their contractual obligations, Gateway's results of operations could be adversely impacted.

Gateway requires a high volume of quality products and components for its PC and Non-PC offerings, substantially all of which are obtained from a limited number of original design manufacturers and suppliers. In some circumstances Gateway maintains single or dual-source vendor relationships, such as with Microsoft for operating system software and Intel and AMD for PC microprocessors. There currently is a lawsuit between AMD and Intel, the outcome of which could impact Gateway's results of operations. If the supply of a key material product or component were delayed or curtailed, Gateway's ability to ship the related product in a timely and cost-effective manner could be adversely affected. Gateway seeks to mitigate a portion of these risks in some cases by maintaining insurance to protect itself against loss of profits due to a vendor's inability to perform due to an insurable property loss. In addition, Gateway seeks to mitigate such risks by having dual sources of supply where appropriate. However, even where multiple vendors are available, Gateway may source from a single vendor to take advantage of volume discounts, for product technical or quality reasons, or to maintain access to certain key components that are at times subject to industry-wide availability and pricing pressures. In cases where Gateway needs to switch to another original design manufacturer or supplier and alternative sources of supply are available, qualification of the sources and establishment of reliable new or additional production with such original design manufacturers or suppliers could result in delays and possible reductions in net sales or increases in cost of goods sold. Gateway also receives market development funding from a few of these suppliers in order to promote or develop markets for computers featuring the supplier's products. If the amount of market development funding were to significantly decline, Gateway's results of operations could be adversely affected.

To minimize some of these risks, Gateway monitors the financial status of certain key original design manufacturers, suppliers and service providers and assesses the likelihood of disruption to the supply of products, components, or services. Certain of its commercial partners are financially weak, and Gateway has established contingency plans to mitigate its financial and operating exposure. However, such plans for any key commercial partner that experiences financial instability may not prevent delays or curtailments of deliveries of key products, components or services, or eliminate Gateway's financial exposure to future costs such as warranty claims or the write-off of receivables from the sale of components to original design manufacturers, which could adversely affect Gateway's future operating results and financial condition.

Many of Gateway's competitors obtain products or components from the same original design manufacturers and suppliers that Gateway utilizes. Gateway's competitors may obtain better pricing and other terms, more favorable allocations of products and components during periods of limited supply, and could limit Gateway's ability to engage in relationships with certain original design manufacturers and suppliers. In addition, certain of Gateway's original design manufacturers and suppliers could decide in the future to not continue

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conducting business with it. Any of these actions by Gateway's competitors, original design manufacturers or suppliers could adversely affect its future operating results and financial condition.

Gateway is dependent on suppliers for trade credit. If such credit is not available, Gateway's liquidity could be adversely affected.

Gateway's ability to obtain trade credit from its suppliers is necessary for its ongoing business operations. Some of its suppliers have restricted the amount and terms of trade credit available to Gateway in response to continued operating losses and the decline in its cash and marketable securities balances. If Gateway continues to experience net losses and see further erosion of its cash balances, trade credit from suppliers could be further limited. While Gateway believes it will have sufficient cash and financial flexibility to meet its operational cash needs for at least the next twelve months, if it is unable to maintain sufficient liquidity, its future results of operations and financial condition would be adversely impacted. See "Item 7. Management's Discussion and Analysis of Financial Condition and Results of Operations—Liquidity and Capital Resources" for more information.

Gateway opened a final assembly facility during 2006 which exposes it to additional financial and operational risk.

To better serve its Professional and Direct customers, Gateway opened a dedicated U.S. final assembly facility in 2006. Gateway assembles configure-to-order desktops, notebooks and servers according to customer specifications at this facility, as well as providing custom imaging services and government compliance certification. This facility is expected to increase Gateway's ability to serve its Professional and Direct customers and improve its cost efficiency. The facility increases Gateway's fixed costs, requires additional systems and controls, and requires additional management oversight and expertise. Should any of these costs or requirements escalate or should anticipated volumes fall below expectations, Gateway's results of operations and financial condition could be adversely impacted.

Gateway's reliance on original design manufacturers or suppliers of key products and components exposes it to potential product quality issues and unanticipated warranty costs that could affect the on-time delivery and performance of its products and services, which could adversely impact operating results.

While outsourcing arrangements may lower its product and operating costs, they also reduce its direct control over production and distribution. If Gateway is unable to ship its products in desired quantities and in a timely manner due to a delay or curtailment of the supply of material products or components, or product quality issues arise due to faulty products or components manufactured by original design manufacturers or suppliers, the market for its products or services could be adversely affected with a resulting reduction in revenues. Gateway's estimated warranty and extended warranty costs are affected by ongoing product failure rates and specific product class failures. If product failure rates, material usage or service delivery costs exceed its estimates due to faulty products or components manufactured by original design manufacturers or suppliers, warranty expenses may increase. In many instances Gateway relies on offshore suppliers, particularly from Asia, for product assembly and manufacturing, and risks associated with transportation, including timely delivery to its primary ports of Los Angeles and Long Beach, California, and other natural or human factors may disrupt the flow of product. If for any reason manufacturing or logistics in any of these locations or the subsequent transportation to the U.S. or other customer locations were disrupted by economic, business, environmental, political, medical, military or terrorist events, Gateway's operations and financial condition could be adversely affected. In addition, Gateway may experience production and financial difficulties if any of its significant original design manufacturers or suppliers suffer financial instability. This includes its likely inability to obtain reimbursement for prepaid warranty costs from certain original design manufacturers, should their financial condition deteriorate. Should such original design manufacturers or suppliers fail to either produce or deliver products as scheduled or to provide prepaid warranty coverage, Gateway's operations and financial condition may be adversely affected.

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Failure to develop and introduce new and technologically advanced products in an industry characterized by short product life cycles could adversely affect Gateway's growth and efforts to sustain profitability.

Gateway's business model depends on bringing new and innovative products to market quickly. The success of its product introductions depends on many factors including the availability of new products, successful quality control and launch readiness efforts, its ability to successfully forecast product demand, training of sales and support personnel, and customer acceptance of new technology. In addition, the introduction of certain new technologies, such as the Microsoft Windows® Vista™ operating system, presents Gateway with uncertainties regarding the speed of customer acceptance, software and hardware compatibility, and manufacturing schedules. If Gateway is unable to successfully forecast demand for new products, it may not properly manage its inventory levels and may have increased exposure to supply shortages, product obsolescence and other supply-related risks.

Short product life cycles resulting from rapid changes in technology and consumer preferences and declining product prices characterize the PC industry. Gateway's internal engineering personnel work closely with product and component suppliers and other technology developers to evaluate the latest developments in PC and Non-PC products. There is no assurance that Gateway will continue to have access to or the right to use new technology, or be successful incorporating such new technology in its products in a timely manner.

The failure to properly manage inventory could adversely affect operating results.

By distributing many of its products directly to its customers prior to its acquisition of eMachines, Gateway historically avoided the need to maintain high levels of finished goods inventory. This minimized costs and allowed Gateway to respond more quickly to changing customer demands and reduced its exposure to the risk of finished product obsolescence. As Gateway increases sales volume into third-party retail channels, managing its inventory effectively has become increasingly important. Third-party retailers may quickly increase orders during periods of product shortages, cancel orders if their inventory is too high, or delay orders in anticipation of new products. Orders also may be adjusted in response to the supply of Gateway's competitors' products and seasonal fluctuations in end-user demand. In addition, Gateway maintains certain component products in inventory. If Gateway is not successful in forecasting component prices or component or product demand, its product costs could be impacted or it could have excess or insufficient inventory of certain components or products and any excess inventory may result in reduced prices and inventory write-downs, which in turn could result in lower gross profits. A decrease in market demand or a decision to increase supply, among other factors, could result in higher finished goods and component inventory levels, and a decrease in value of this inventory could have a negative effect on Gateway's results of operations. Although Gateway's management believes the company's inventory and related reserve provisions are adequate, given the rapid and unpredictable pace of product obsolescence in the PC industry, no assurance can be given that Gateway will not incur significant additional inventory and related charges. In addition, by purchasing component parts on behalf of original design manufacturers, Gateway has increased its credit risk with these original design manufacturers.

The failure to attract, retain and motivate key personnel could have a significant near-term adverse impact on Gateway's operations.

Gateway's ability to attract, retain and motivate employees and maintain employee morale has been adversely impacted by a number of factors, including workforce reductions, the closure of facilities and a competitive PC business environment. Gateway has experienced, and may continue to experience, turnover in senior management and in the general workforce, which may disrupt business operations, internal controls, and relationships with commercial partners and customers. Turnover, particularly among senior management, can also create distractions and cause operational inefficiencies as replacement personnel become familiar with its business and operations. In addition, manpower in certain areas may be constrained, which could lead to disruptions over time. There can be no assurance that Gateway will continue to successfully attract or retain the management it needs, or be able to maintain an optimal workforce size. Any inability to attract, retain or motivate such personnel or address manpower constraints as needed could materially adversely affect its future operating results, internal controls and financial condition.

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Gateway has outsourced operations in countries outside of the U.S. and changes in the political environment, economic policies and other factors within those countries or the U.S. could adversely affect its business.

Gateway has outsourced a substantial portion of its manufacturing operations to countries in Asia, Eastern Europe, and Mexico. A change in these countries' economic or regulation policies could adversely affect business and economic conditions in the affected country generally and could negatively impact the cost-saving benefits of Gateway's outsourced operations overseas. While Gateway's contract obligations are typically in U.S. dollars, changes in currency exchange rates could impact its suppliers and increase prices. Changes in Chinese Yuan renminbi to United States dollar exchange rate could increase its costs for products and components sourced from China. Any political instability could also change the present satisfactory legal environment for us through the imposition of restrictions on foreign ownership, repatriation of funds, adverse labor laws, and the like. Further, risks associated with transportation and other natural or human factors, including disease epidemics, may disrupt operations in and the flow of products from certain countries. Gateway also has outsourced workers in countries outside of the U.S. in technical support call centers, repair centers, and refurbishment centers. These outsourced operations present Gateway with similar economic and political risks. The political climate in the U.S. also could change, which could adversely affect Gateway's ability to maintain or create low-cost operations outside the U.S.

Environmental laws and regulations and unforeseen costs could impact Gateway's future earnings.

Production and marketing of products in certain states and countries may subject Gateway to environmental and other regulations. Gateway also could face significant costs and liabilities in connection with product take-back legislation, which provides customers the ability to return product at the end of its useful life and places financial and other responsibility for environmentally safe collection, recycling, treatment and disposal with Gateway. Gateway also faces increasing complexity in its product design and procurement and operations as Gateway adjusts to new and upcoming requirements relating to the materials composition of its products, including the restrictions on lead and certain other substances that apply to specified electronics products marketed in the European Union as of July 1, 2006. The European Union has also finalized the *Waste Electrical and Electronic Equipment Directive*, which makes producers of electrical goods, including computers and printers, financially responsible for specified collection, recycling, treatment and disposal of past and future covered products. There is substantial complexity associated with compliance with these new regulations and the costs of implementation are not easily quantifiable. Compliance also necessitates its reliance on the representations made by suppliers as to material composition; while such representations are believed to be accurate, Gateway could face significant costs and liabilities if the representations prove to not be accurate. Furthermore, Gateway must rely on its suppliers' ability to respond to environmental requirements with compliant products and documentation in a timely manner.

Similar laws and regulations have been or may be enacted in other states and countries. Other environmental regulations may require Gateway to reengineer its products to utilize components which are more environmentally compatible and such reengineering and component substitution may result in additional costs to Gateway. Although Gateway does not anticipate any material adverse effects based on the nature of its operations and the effect of such laws, there is no assurance that such existing laws or future laws will not have a material adverse effect on Gateway.

Gateway is subject to seasonality which can make it difficult to forecast results of operations and anticipate near term developments.

Gateway's revenues and operating margins vary among products, distribution channels and the seasonal buying habits of its customers. Historically revenues in the Retail segment are seasonally higher during the second half of the year, and Professional segment revenues are seasonally higher in the second and third quarters. Consequently, the overall operating margins of Gateway in any given period will depend, in part, on the product, geographic and channel mix reflected in that period's net sales, as well as seasonality factors related to the time

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of the year. In addition, Gateway typically experiences an increase in sales activity near quarter-end. Developments late in a quarter, such as lower-than-anticipated demand for Gateway's products or late arriving components and scheduling/production delays at its manufacturing or logistics partners, fluctuations in product, geographic and channel mix, and the effect of seasonality on its sales and operating margins can have significant adverse impacts on Gateway and its results of operations and financial condition for a given reporting period.

Expansion into international markets exposes Gateway to increased risks, which could adversely impact operating results.

Gateway has expanded sales of PCs and certain Non-PC products into international markets. International sales are subject to certain inherent risks including unexpected changes in regulatory requirements and tariffs, including antidumping penalties, risks in hedging for foreign currency fluctuations for non-U.S. dollar sales, difficulties in managing foreign operations, legal remedies that can affect accounts receivable collection and potentially adverse tax consequences. In addition, given that its products in international markets are sold primarily through a small number of third-party retail partners, Gateway's business and financial results could be adversely affected if the financial condition of any of these retailers weakens or if they were to cease or significantly reduce the distribution of its products. For those international sales not denominated in U.S. dollars, any strengthening of the U.S. dollar relative to the currencies of other countries into which Gateway sell its products and services could make its products and services more expensive, thereby reducing the price-competitiveness of its products. Should any of these difficulties arise, its results of operations and financial condition could be adversely impacted.

War, terrorist acts and other political and economic uncertainties may adversely affect Gateway's operating results.

War and the related political and economic uncertainties, terrorist attacks, national and international responses to terrorist attacks, and other acts of hostility could materially adversely affect demand for Gateway's products and disrupt its supply chain or customer fulfillment logistics or operations, resulting in an adverse impact on its future operating results and financial condition.

If Gateway cannot sustain profitability and Gateway incurs significant net losses or negative cash flows, the business could fail.

Gateway experienced net losses in the years ended December 31, 2003 and 2004 of \$515 million and \$568 million, respectively. While Gateway reported net income of \$9.6 million for the year ended December 31, 2006 and \$6.1 million for the year ended December 31, 2005, approximately \$35 million and \$41 million, respectively, was attributable to the Marketing, Development and Settlement Agreement with Microsoft, which expires in the fourth quarter of 2008 and Gateway cannot guarantee its future profitability, and additional significant net losses would materially adversely affect Gateway's financial condition, results of operations and cash flows.

Its cash and marketable securities balances have declined since the first quarter of 2004 from historically higher levels due to the eMachines acquisition, restructuring its company, working capital usage in support of expanding its Retail business, and other operating, investing and financing activities. Cash and marketable securities balances declined materially from December 31, 2005 to December 31, 2006. Gateway may be unable to generate positive cash flow, which would result in declining cash and marketable securities balances. Gateway may be required to raise additional cash through additional debt or equity instruments. Gateway's management believes Gateway will have sufficient cash and financial flexibility to meet its operational cash needs for the next twelve months. If it is unable to maintain sufficient liquidity or raise additional capital, its future results of operations and financial condition would be adversely impacted.

Gateway's failure to protect customer data could adversely affect our sales and reputation.

There have been a number of instances in which personal information maintained by companies has been lost or stolen. Gateway collects and maintains large amounts of customer data in the normal course of its

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business, and Gateway's service providers collect and maintain customer data in the course of providing services to customers on Gateway's behalf. Gateway has policies and procedures in place to protect against inadvertent disclosure of customer data by it and its suppliers. It also proactively searches and seeks to protect against intrusions into its infrastructure to prevent the theft of customer data. Although Gateway believes it has effective policies, procedures and technology to prevent the disclosure of customer data, the loss or theft of customer data could adversely affect Gateway's sales and reputation with its customers, as well as expose Gateway to potential damages and costs that could be material.

If Gateway does not maintain its reputation and expand its name recognition, Gateway may lose customers which would adversely impact its financial results.

Developing and maintaining awareness of its Gateway and eMachines brand names is critical to achieving widespread acceptance of its PC and Non-PC offerings. Promotion and enhancement of its brand will depend largely on whether Gateway cost-effectively provides reliable and desirable products and services to customers and the effectiveness of its marketing efforts. Currently, third-party retailers are often its first points of contact with consumers and these retailers provide much of its product advertising as Gateway has reduced its internal spending on marketing. If these retailers reduce or cease advertising its products, Gateway may need to increase its own sales and marketing expenses to create and maintain brand awareness among potential consumers. If customers do not perceive Gateway's products to be of high quality, its brand names and reputation could be harmed, which could adversely impact its financial results.

Gateway's internal control over financial reporting could be adversely affected by a material weakness in its internal controls. If not corrected, its operating results and stock price could be adversely affected.

During the course of the 2006 year-end close process, Gateway's management examined Gateway's processes relating to its receipt of components from original equipment manufacturers (OEMs) and sale of components to original design manufacturers (ODMs). As a result of that evaluation, management concluded that Gateway did not adequately design controls to ensure the timely accrual of liabilities to OEMs, recording of receivables from ODMs and receipt of inventory (see Item 9A). While Gateway continues to take steps to remediate this material weakness, there can be no assurance that Gateway will be able to completely remediate it such that management will be able to conclude that its internal control over financial reporting is effective. The existence of a significant deficiency or a material weakness could result in errors in Gateway's financial statements that could result in a restatement, cause Gateway to fail to timely meet its reporting obligations and cause investors to lose confidence in its reported financial information, leading to a decline in Gateway's stock price.

Item 1B. Unresolved Staff Comments

None.

Item 2. Properties

The following are Gateway's principal administrative and sales offices, operational facilities and support centers in the following locations:

Facilities	Square Footage	Owned or Leased	Description / Property Use	Segment Use
Irvine, California	98,000	Leased	Corporate headquarters	All segments
Irvine, California	147,000	Leased	Warehouse and office space	All segments
North Sioux City, South Dakota	352,000	Owned	Customer sales and support center; administration	All segments
North Sioux City, South Dakota	15,000	Leased	Records storage	All segments
La Vergne, Tennessee	94,000	Leased	Assembly	Professional, Direct

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Gateway continues to sublease or actively market to sublease or terminate approximately 22 remaining retail locations throughout the United States, as a result of the closure of all of its retail stores in April 2004. Gateway also continues to lease, sublease and actively market for sale, lease, or sublease office and distribution facilities in Lake Forest, San Diego and Poway, California; Lakewood and Colorado Springs, Colorado; Kansas City, Missouri, North Sioux City, South Dakota, and Hampton, Virginia.

Gateway believes that its administrative and sales offices, operational facilities and support centers will be adequate for its business needs in the foreseeable future.

Item 3. Legal Proceedings

Gateway is a party to various lawsuits, claims, including assertions of patent infringements, investigations and administrative proceedings that arise in connection with its business, including those identified below. Gateway evaluates such matters on a case by case basis, and its policy is to vigorously contest any such claims it believes are without merit.

Litigation

Rattner v. Snyder, et al. is a derivative action filed on September 6, 2006, in California State Superior Court, County of Orange, against Gateway as a nominal defendant and against individual members of Gateway's board of directors. The suit alleges that Board members breached their fiduciary duties in connection with the Gateway's September 1, 2006 announcement that it had rejected an earlier offer by shareholder Lap Shun "John" Hui to acquire Gateway's retail operations for approximately \$450 million. The complaint seeks unspecified damages and declaratory relief. On November 13, 2006, Gateway filed a motion for an order compelling plaintiff to furnish a bond, pursuant to California Corp. Code § 800(c), and the court has yet to rule on Gateway's motion. The parties have stipulated that the director defendants need not appear in the matter or otherwise respond to the complaint until after a demand-futility motion to be filed by Gateway is resolved.

Lucent Technologies, Inc. v. Gateway, Inc. is a suit filed on June 6, 2002 in the United States District Court for the Eastern District of Virginia, which was subsequently transferred to the United States District Court for the Southern District of California, asserting that Gateway infringes seven patents owned by Lucent Technologies, Inc. On or about February 26, 2003, Microsoft intervened in the action, seeking to challenge Lucent's allegations with respect to five of the seven patents. In addition, on April 8, 2003, Microsoft filed an action against Lucent in the United States District Court for the Southern District of California. The suit seeks declaratory judgment that Microsoft products do not infringe patents held by Lucent, including the five patents upon which Microsoft based its intervention in the action Lucent brought against Gateway. On February 20, 2003, Lucent also sued Dell Inc. in the United States District Court for the District of Delaware on six patents, all of which are included in Microsoft's declaratory judgment action, and several of which are asserted by Lucent against Gateway. The suit against Dell was subsequently transferred to the United States District Court for the Southern District of California, where all three actions have been consolidated for discovery purposes. Lucent subsequently filed amended complaints against Dell and Gateway, respectively, asserting the same patents against each company. Through its amendments, Lucent asserted one additional patent against Dell and four additional patents against Gateway. All of the patents added through amendment are at issue in the Microsoft declaratory judgment action. The Court began conducting a Markman hearing on the asserted patents in August 2003 and conducted over 30 days of hearings before concluding the Markman hearing in September 2005. In September 2005, the Court also granted a summary judgment of invalidity with respect to one of the Lucent patents asserted against Gateway. Discovery is complete. The three actions have been consolidated into five separate trials, in which a different group of patents will be tried to each jury. The first of those trials involved Microsoft only, and was related to audio patents not asserted against Gateway. On February 22, 2007, a jury returned a verdict of approximately \$1.5 billion against Microsoft. Microsoft is expected to appeal. The first trial that involves Gateway is scheduled to begin on March 19, 2007, with three additional trials expected to occur in 2007 and possibly 2008.

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Dvorchak v. eMachines, Inc., et al. is a shareholder class action against eMachines, Inc. and others filed in November 2001, in California State Superior Court, County of Orange, relating to a 2001 transaction in which eMachines, which was then a public company, was taken private. The action originally sought to enjoin eMachines' merger with Empire Acquisition Corp. (the "Merger") to effectuate taking eMachines private. The court denied the requested injunction on December 27, 2001, allowing the consummation of the Merger. After the Merger, plaintiffs filed amended complaints seeking unspecified monetary damages and/or rescission relating to the negotiations for and terms of the Merger through allegations of breaches of fiduciary duties by eMachines, its board members prior to the Merger, and certain of its officers. The court granted class certification on August 25, 2003. Dispositive motions filed by the defendants were heard and denied by the Court in August 2004 and August 2005. No trial date has been set, but the trial is currently anticipated to occur sometime in 2007.

In accordance with SFAS No. 5, "Accounting for Contingencies," Gateway reserves for a legal liability when it is both probable that a liability has been incurred and the amount of the loss can be reasonably estimated. At least quarterly Gateway reviews and adjusts these reserves to reflect the impacts of negotiations, settlements, rulings, advice of legal counsel and other information and events pertaining to a particular case. The ultimate outcome of such matters cannot presently be determined or estimated. Gateway's management believes that Gateway has sufficiently reserved for legal matters and that the ultimate resolution of pending matters will not have a material adverse impact on Gateway's consolidated financial position, operating results or cash flows. However, the results of legal proceedings cannot be predicted with certainty. Should Gateway fail to prevail in current legal matters or should one or more of these legal matters be resolved against Gateway, Gateway could be required to pay substantial monetary damages or, if injunctive relief is granted, may be prohibited from selling one or more of its products and, in either case, its operating results and cash flows could be materially adversely affected.

Item 4. *Submission of Matters to a Vote of Security Holders*

Not applicable.

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PART II

Item 5. *Market for Registrant's Common Equity, Related Stockholder Matters and Issuer Purchases of Equity Securities*

Market Information

Gateway common stock is listed on the New York Stock Exchange under the trading symbol "GTW." The following table sets forth the quarterly high and low closing prices per share for Gateway's common stock in 2005 and 2006:

	<u>High</u>	<u>Low</u>
2005:		
1st quarter	\$5.85	\$3.95
2nd quarter	\$4.16	\$2.85
3rd quarter	\$4.08	\$2.44
4th quarter	\$3.16	\$2.48
2006:		
1st quarter	\$2.93	\$2.15
2nd quarter	\$2.36	\$1.53
3rd quarter	\$2.09	\$1.30
4th quarter	\$2.17	\$1.60

Holders of Record

As of February 20, 2007, there were 6,862 holders of record of our common stock. There were no issued and outstanding shares of the Class A Common Stock as of such date.

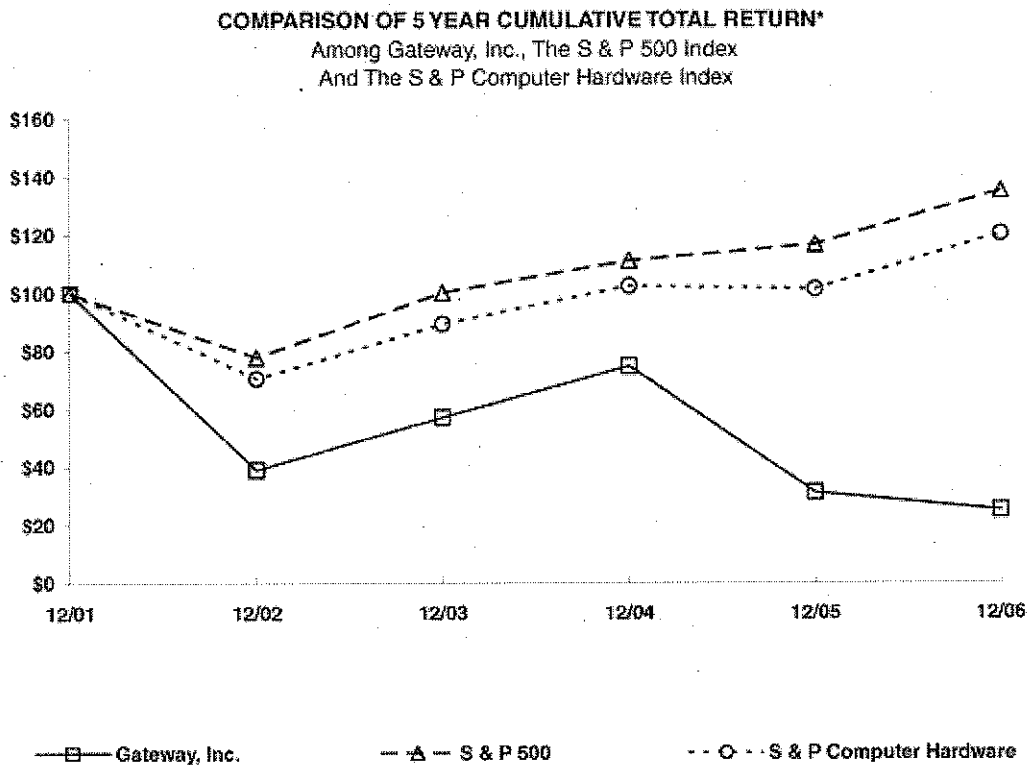
Dividends

Gateway's management believes the best use of cash is to fund internal growth and for general corporate purposes. As a result, it has not declared any cash dividends on its common stock since it was first publicly registered and does not anticipate paying any cash dividends on its common stock in the foreseeable future. In addition, Gateway's credit agreement restricts its ability to pay dividends on its common stock.

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Stock Performance Graph

The following graph shows the cumulative total return assuming the investments of \$100 from December 31, 2001 through December 31, 2006 (and the reinvestment of dividends thereafter) in each of our common stock, the S&P 500 Index and the S&P Computer Hardware Index. Past financial performance should not be considered a reliable indicator of future performance, and investors should not use historical trends to anticipate results or trends in future periods.



* \$100 invested on 12/31/01 in stock or Index-including reinvestment of dividends. Fiscal year ending December 31.

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Issuer Purchases of Equity Securities

The following table sets forth information with respect to purchases by Gateway of its equity securities registered pursuant to Section 12 of the Exchange Act during 2006:

Period	(a) Total Number of Shares of Common Stock Acquisition	(b) Average Price Paid Per Share of Common Stock	(c) Total Number of Shares of Common Stock Purchased as Part of Publicly Announced Plans or Programs	(d) Maximum Number (or Approximate Dollar Value of Shares of Common Stock that May Yet Be Purchased Under the Plans or Programs
January 1-31, 2006	996,383	\$ 2.70	—	—
February 1-28, 2006	—	—	—	—
March 1-31, 2006	—	—	—	—
April 1-30, 2006	—	—	—	—
May 1-31, 2006	—	—	—	—
June 1-30, 2006	167,665	\$ 1.67	—	—
July 1-31, 2006	—	—	—	—
August 1-31, 2006	—	—	—	—
September 1-30, 2006	—	—	—	—
October 1-31, 2006	122,224	1.84	—	—
November 1-30, 2006	—	—	—	—
December 1-31, 2006	—	—	—	—
Total	1,286,272	\$ 2.48	—	—

The 996,383 shares of common stock represents the value of taxes withheld on the aggregate vesting of 2,146,426 shares of restricted stock originally issued in connection with the eMachines' acquisition in March 2004. Gateway repurchased 167,665 shares of common stock in a private transaction from a Gateway executive at a price equal to the market price on June 5, 2006, the date of purchase. The 122,224 shares of common stock represents the value of taxes withheld on the vesting of employee restricted stock on October 4, 2006.

Item 6. Selected Consolidated Financial Data

The following historical data was derived from Gateway's audited consolidated financial statements. This financial data as of December 31, 2006 and 2005 and for the years ended December 31, 2006, 2005 and 2004 should be read in conjunction with Item 8 "Consolidated Financial Statements and Supplementary Data" of this Annual Report and in conjunction with Item 7 "Management's Discussion and Analysis of Financial Condition and Results of Operations" of this Annual Report. The information below is not necessarily indicative of the results of future operations.

	For the years ended December 31,				
	2006	2005	2004 (a)	2003	2002
Consolidated Statements of Operations Data (in thousands, except per share data):					
Net sales	\$3,980,803	\$3,854,061	\$3,649,734	\$3,402,364	\$4,171,325
Net income (loss) (b)	\$ 9,643	\$ 6,161	\$ (567,618)	\$ (514,812)	\$ (297,718)
Net income (loss) attributable to common shareholders	\$ 9,643	\$ 6,161	\$ (475,476)	\$ (525,950)	\$ (309,041)
Net income (loss) per common share:					
Basic	\$ 0.03	\$ 0.02	\$ (1.31)	\$ (1.62)	\$ (0.95)
Diluted	\$ 0.03	\$ 0.02	\$ (1.45)	\$ (1.62)	\$ (0.95)

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	As of December 31,				
	2006	2005	2004 (a)	2003	2002
Consolidated Balance Sheet Data (in thousands):					
Cash and marketable securities	\$ 416,335	\$ 585,688	\$ 588,330	\$1,051,456	\$1,021,847
Total assets	\$1,656,235	\$1,921,066	\$1,771,787	\$2,028,438	\$2,509,407
Senior convertible notes	\$ 300,000	\$ 300,000	\$ 300,000	\$ —	\$ —
Series C redeemable convertible preferred stock	\$ —	\$ —	\$ —	\$ 197,720	\$ 195,422
Stockholders' equity	\$ 269,008	\$ 255,274	\$ 245,037	\$ 722,018	\$1,246,518

- (a) Results for 2004 reflect the inclusion of eMachines' activity subsequent to March 11, 2004.
 (b) Net income (loss) includes certain restructuring, transformation, integration and other charges of \$0.5 million, \$13 million, \$478 million, \$192 million, and \$99 million for 2006, 2005, 2004, 2003, and 2002, respectively.

Item 7. Management's Discussion and Analysis of Financial Condition and Results of Operations

The following discussion should be read in conjunction with the Consolidated Financial Statements and the related notes that appear elsewhere in this document.

This Annual Report includes forward-looking statements made based on current management expectations. These statements are not guarantees of future performance and actual outcomes may differ materially from what is expressed or forecasted. Factors that could cause future results to differ from Gateway's expectations include the factors described in Item 1A "Risk Factors" of this Annual Report or that are otherwise described from time to time in our reports filed with the Securities Exchange Commission after this Annual Report. We assume no obligation to update any forward-looking statements to reflect events that occur or circumstances that arise after the date as of which they are made.

Management's discussion and analysis that follows is designed to provide information that will assist readers in understanding our consolidated financial statements, changes in certain items in those statements from year to year and the primary factors that caused those changes and how certain accounting principles, policies and estimates affect our financial statements.

Overview

Since its founding in 1985, Gateway has focused on marketing PCs and related products and services at a price that represents value to consumers, businesses, government offices and educational institutions.

We manage our business through our three major business segments: Retail (including International), Professional and Direct. Our strengths include our strong brand name recognition, our value-based product lines, and our ability to maneuver quickly and react to product development trends in the rapidly changing PC industry.

Some of the key developments and achievements for 2006 include:

- *Net income and PC unit sales*—we posted net income of \$9.6 million or \$0.03 per share for the year ended December 31, 2006. Total PC unit sales of five million were up 12% over 2005.
- *Continued Cost Structure Improvements*—SG&A expenses for the year were \$309 million (including \$0.5 million in restructuring, transformation and integration expenses), compared with \$364 million in 2005 (including \$13 million in restructuring, transformation and integration expenses). In the fourth quarter we announced plans to further reduce corporate SG&A through a cost reduction program that will yield \$30-35 million in 2007. As a result of further activities, we believe we will achieve cost reductions that will exceed \$30-35 million.

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- *Notebook and Display Sales Growth*—in 2006, we continued to experience sales momentum with our notebook products and flat panel displays. Notebook unit sales were up 48% in 2006 compared with 2005 and display sales were up 13% over 2005 sales.
- *Continued Retail and International Expansion*—2006 saw continued strong contributions from U.S. Retail as PC unit sales were up by 22% overall, paced by surging notebook and display sales. Notebook unit sales were up 63% and flat panel display sales were up by nearly 60% over 2005. Based on NPD data, Gateway was the fastest growing notebook brand in U.S. Retail among the top-five vendors. International retail sales were up in 2006 as well. Gateway exited the year with more than 3,400 stores carrying Gateway and eMachines products in France, Japan, Mexico and the United Kingdom.
- *New Products*—Gateway introduced a number of new products during 2006, including its flagship Gateway FX530 desktop PC line for digital enthusiasts, which has been widely acclaimed for delivering maximum performance and setting new standards for value in this high-end category. With this platform, Gateway became the first major PC OEM to offer warranty support for factory over-clocked processors. Gateway also built on the success of its award-winning 21-inch wide LCD display with a complete line of wide displays at 19-, 22- and 24-inches. Gateway also introduced a number of new notebook products for all sales channels featuring the latest mobile technology. For Professional customers, Gateway's server line-up was redesigned, offering a new industrial design, enhanced serviceability and remote system management. The company also introduced a new storage area network (SAN) product, which provides enterprise-class storage at an entry-level price without sacrificing performance or reliability.
- *New CEO*—in September 2006, Gateway named Ed Coleman as CEO, replacing Chairman Rick Snyder, who served as interim CEO for most of 2006. A 30-year veteran of the technology industry, Coleman has broad-based experience that includes sales and marketing, operations, IT services and finance roles with some of the world's most successful technology companies.
- *Board of Directors*—in December 2006, Gateway enhanced its Board of Directors by appointing Scott Galloway to the Board. Mr. Galloway, a clinical associate professor at NYU's Stern School of Business and managing member of Firebrand Partners, brings a strong marketing perspective to the Board.
- *Award-winning North America-based Tech Support*—in 2006, Gateway transitioned all of its customer care operations and support for customers in the U.S. and Canada to North America. As evidenced by the company's improved performance in a number of third-party service-related studies, this move is paying off. In fact, in the two most recent Technology Business Research (TBR) Corporate IT Buying Behavior and Customer Satisfaction Studies for both desktop and notebook PCs, Gateway earned the number one designation and our "North America-based" approach to customer care was cited as a key factor in both studies.

We continue to face a variety of challenges and opportunities inherent within the PC industry which is characterized by rapid change, evolving customer demands and intense competition. Key challenges include increasing demand for our products in a highly competitive market, increasing revenue, lowering costs, managing our supply chain and increasing gross profit. See Item 1A "Risk Factors".

Critical Accounting Policies and Estimates

Management's Discussion and Analysis of Financial Condition and Results of Operations contains a discussion of Gateway's consolidated financial statements, which have been prepared in accordance with accounting principles generally accepted in the United States of America. The preparation of financial statements and related disclosures in conformity with generally accepted accounting principles and Gateway's discussion and analysis of our financial condition and results of operations requires Gateway's management to make judgments, assumptions and estimates that affect the amounts reported in our consolidated financial statements and accompanying notes.

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Management believes the following are critical accounting policies whose application has a material impact on Gateway's financial presentation. That is, they are both important to the portrayal of Gateway's financial condition and results, and they require management to make judgments and estimates about matters that are inherently uncertain.

Revenue Recognition

Gateway recognizes revenue on PCs, servers and Non-PC products when persuasive evidence of an arrangement exists, delivery has occurred, the sales price is fixed and determinable, and collectibility is reasonably assured. Revenue from training services is recognized as the services are provided. Revenue from Internet access, web portal, and security services provided by third parties is recognized as the services are provided based on subscriber counts reported to us by the service providers. If the actual subscriber counts or the economics associated with these subscriber counts prove to be more or less than originally reported by the service providers, we may be required to adjust revenue. In the fourth quarter of 2002, America Online, Inc. ("AOL") unilaterally recomputed payments it had made in 2001 and the first half of 2002 and withheld the claimed overpayments from amounts currently owed to us. We disputed AOL's retroactive adjustment and reached a settlement in November 2004 for \$2.5 million related to the contested period and an additional \$1.6 million for subsequent periods through 2004. This was recognized as revenue in 2004. Revenue from the sale of other services rendered by third parties, such as installation services, is generally recognized when such services are performed.

Gateway offers its customers an option to purchase extended warranties. Revenue related to sales of extended warranties sold on behalf of third-parties is recognized at the time of sale, net of amounts due to the third-party. Revenue from sales of extended warranties where Gateway is the legal obligor is deferred and recognized on a straight-line basis over the warranty service period.

Gateway records reductions in revenue in the current period for estimated future product returns and estimated rebate redemption rates related to current period sales. Management analyzes historical returns, current trends, changes in customer demand and acceptance of our products when evaluating the adequacy of the sales returns allowances in any accounting period. Management also analyzes historical rebate redemption rates, current trends and the interrelationship of these rates with the current rebate dollar amounts in evaluating rebate allowances. If actual returns exceed estimated returns or if actual rebate redemptions exceed estimates, we would be required to record additional reductions to revenue which would affect earnings in the period the adjustments are made. Gateway also records reductions to revenue for estimated commitments related to other customer and sales incentive programs. This includes, among other things, trade-ins and referral credits. Future market conditions and product transitions may require us to increase customer incentive programs that could result in incremental reductions of revenue at the time such programs are offered, which would affect earnings in the period the adjustments are made.

Gateway records revenue net of sales or valued added taxes levied by governmental authorities. Such taxes are considered current liabilities and included within accrued expenses until paid.

Allowance for Doubtful Accounts

Gateway maintains an allowance for doubtful accounts for estimated losses resulting from the inability of our customers to make required payments. The estimate is based on management's assessment of the collectibility of specific customer accounts and includes consideration of the creditworthiness and financial condition of those specific customers. We record an allowance to reduce the specific receivables to the amount that is reasonably believed to be collectible. We also record an allowance for all other trade receivables based on multiple factors including historical experience with bad debts, the general economic environment, the financial condition of our customers, and the aging of such receivables. If there is a deterioration of a major customer's financial condition or we become aware of additional information related to the credit worthiness of a major

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customer, or if future actual default rates on trade receivables in general differ from those currently anticipated, we may have to adjust our allowance for doubtful accounts, which would affect earnings in the period the adjustments are made.

Inventory Valuation

The business environment in which Gateway operates is subject to rapid changes in technology and customer demand. We record write-downs for components and products which have become obsolete or are in excess of anticipated demand or net realizable value. We perform an assessment of inventory each quarter, which includes a review of, among other factors, inventory on hand and forecast requirements, product life cycle (including end of life product) and development plans, component cost trends, product pricing and quality issues. Based on this analysis, we record an adjustment for excess and obsolete inventory. Gateway may be required to record additional write-downs if actual demand, component costs or product life cycles differ from estimates, which would affect earnings in the period the write-downs are made.

Receivables from Suppliers

Gateway purchases selected components from suppliers and resells the components to original design manufacturers to incorporate into products being manufactured for Gateway. The receivable from these sales of the components is recorded as "Receivables from suppliers". If substantial uncertainty regarding the collectibility of these receivables is noted, an appropriate reserve may be required, which would affect earnings in the period the uncertainty is identified.

Internal-use Software

Gateway capitalizes only those direct costs associated with the actual development or acquisition of computer software for internal use, including costs associated with the design, coding, installation and testing of the system. Costs associated with preliminary development, such as the evaluation and selection of alternatives, as well as training, maintenance and support are expensed as incurred. Gateway is currently migrating to a new enterprise resource planning system as well as new order-capture and back-end service and support systems. A significant change to the planned use of internal-use software could result in a material impairment charge or a change in the estimated depreciable life which could result in increased depreciation expense in the reporting period that the change was made.

Warranty Provision

Gateway provides standard warranties with the sale of products. The estimated cost of providing the product warranty is recorded at the time revenue is recognized. We maintain product quality programs and processes, including actively monitoring and evaluating the quality of suppliers. Estimated warranty costs are affected by ongoing product failure rates, specific product class failures outside of experience and material usage and service delivery costs incurred in correcting a product failure or in providing customer support. If actual product failure rates, material usage or service delivery costs differ from the estimates, revisions to the estimated warranty liability would be required and would affect earnings in the period the adjustments are made.

Restructuring

Gateway has engaged and may continue to engage in restructuring actions which require our management to make significant estimates related to realizable values of assets made redundant or obsolete, expenses for severance and other employee separation costs, lease cancellation and other exit costs, and estimates of future rental income that may be generated through the subleasing of excess facilities. Should the actual amounts differ from our estimates, the amount of the restructuring charges could be materially impacted. For a description of our restructuring actions, refer to our discussion of restructuring charges in the "Results of Operations" section.

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Long-lived Asset Impairments

Gateway reviews long-lived assets for impairment whenever events or changes in circumstances indicate that the carrying amount of an asset may not be recoverable. This process requires management to make assumptions and estimates related to estimated future net cash flows to be generated and used by an asset or asset group as well as the expected or future use of such assets and/or their estimated future useful lives. Actual results could differ from the assumptions and estimates used and a significant change to the planned use of an asset or asset group could result in a change of the useful life in a given reporting period.

Taxes on Earnings

Gateway records a tax provision or benefit for the anticipated tax consequences of our reported results of operations. The provision for (benefit from) income taxes is computed using the liability method, under which deferred tax assets and liabilities are recognized for the expected future tax consequences of temporary differences between the financial reporting and tax bases of assets and liabilities. We record a valuation allowance to reduce our deferred tax assets to the amount that we believe is more likely than not to be realized. We consider our ability to carry back historical losses, cumulative losses in recent years, forecasted earnings and future taxable income and feasible tax planning strategies in determining the need for and amount of a valuation allowance. If we determine that it is more likely than not that our net deferred tax assets will be realized, our valuation allowance would be reversed, resulting in a positive adjustment to earnings in the period such determination is made. Gateway expects to maintain a full valuation allowance on potential future tax benefits and generally to record no tax benefit until an appropriate level of profitability is sustained.

Litigation

Gateway is currently involved in certain legal proceedings (see Note 5 to the Consolidated Financial Statements). When a loss is considered probable in connection with litigation or governmental proceedings and the loss amount can be reasonably estimated within a range, we record the minimum estimated liability related to the claim if there is no best estimate in the range. As additional information becomes available, we assess the potential liability related to the legal proceedings and revise those estimates. Revisions in estimates of the potential liability could materially impact our results of operations in the period of adjustment.

Non-Amortized Intangible Assets Including Goodwill

On March 11, 2004, Gateway acquired eMachines, a privately-held PC company, in a transaction valued at approximately \$262 million. The acquisition combined Gateway's Professional and Consumer (now called "Direct") businesses, scale and cash availability with eMachines' low cost structure, profitability, PC market strength, third-party retail network, and international presence. These factors contributed to a purchase price in excess of the fair value of eMachines' net tangible and intangible assets acquired and, as a result, Gateway recorded goodwill of \$156 million. Gateway also recorded \$50 million in intangible assets related to the eMachines trade name. These intangible assets are not amortized but are reviewed for impairment annually during the fourth quarter or whenever events or circumstances indicate an event of impairment may have occurred or exist. Gateway's fourth quarter review process utilizes multiple methods to estimate fair value based on a discounted future cash flow approach that relies on estimates about Gateway's future revenues (based on assumed market segment growth rates) and costs, discounted at appropriate rates based on Gateway's weighted average cost of capital. Future revenue and cost estimates are based on historical data, various internal estimates and a variety of external sources, and are developed as part of our routine long-range planning process. Gateway's fourth quarter of 2006 assessment supported the conclusion that no impairment of non-amortized intangible asset, including goodwill, existed as of December 31, 2006. A significant change in Gateway's Retail business could result in a material impairment of these assets.

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Microsoft Agreement

Gateway receives funding on a quarterly basis through 2008 from Microsoft under a Marketing, Development and Settlement Agreement (the "Agreement"). The Agreement requires that we use a substantial majority of the \$144 million proceeds to fund various marketing and promotional initiatives, including advertising, sales training and consulting, as well as the research, development and testing of new Gateway products that run Microsoft products and releases Microsoft from all antitrust claims Gateway had made. Although the Agreement contains future marketing and development as well as historical legal components, the relative fair value of these components could not be comprehensively determined. As a result, these two components were not bifurcated for purposes of income statement presentation. We recognize the funding received under this arrangement as a reduction of operating expenses under the line item "Microsoft benefit" upon the later of qualifying spend or cash receipt. If the company fails to incur sufficient qualifying spend or if Microsoft fails to fund such spend on a timely basis, this could result in a material adverse impact to the financial results because Gateway would not be able to record the benefit.

Results of Operations

The following table summarizes Gateway's consolidated results of operations and net sales for the past three years (in thousands):

	2006	Percentage Change	2005	Percentage Change	2004
Net sales	\$3,980,803	3.3%	\$3,854,061	5.6%	\$3,649,734
Gross profit	\$ 255,361	(20.8)%	\$ 322,438	5.0%	\$ 307,072
Percentage of net sales	6.4%		8.4%		8.4%
Selling, general and administrative expenses	\$ 308,738	(15.1)%	\$ 363,578	(60.0)%	\$ 909,050
Percentage of net sales	7.8%		9.4%		24.9%
Microsoft benefit	\$ 34,500	(14.8)%	\$ 40,500	100.0%	—
Percentage of net sales	0.9%		1.1%		—
Operating loss*	\$ (18,877)	(2,849.5)%	\$ (640)	99.9%	\$ (601,978)
Percentage of net sales	(0.5)%		(0.0)%		(16.5)%
Net income (loss)	\$ 9,643	56.5%	\$ 6,161	101.1%	\$ (567,618)
Units shipped	5,013	12.0%	4,476	26.8%	3,530

* Includes \$0.5 million, \$13 million, and \$478 million in 2006, 2005, and 2004, respectively, of restructuring, transformation and integration charges. See the "Restructuring Activities" section below for additional information.

Net Sales

2006 vs. 2005

The \$127 million increase in 2006 net sales as compared to 2005 was primarily due to growth in our Retail segment (\$381 million), which includes international, partially offset by sales declines in the Direct segment (\$163 million) and Professional segment (\$91 million).

See "Segment Performance" below for further discussion of net sales performance on a segment basis.

2005 vs. 2004

The \$204 million increase in 2005 net sales compared to 2004 was primarily due to growth in our Retail segment (\$873 million), partially offset by net sales declines in the Direct segment (\$541 million) primarily resulting from the closure of our Gateway retail stores in April 2004 (which contributed \$391 million to net sales in 2004), in addition to less promotion and advertising of low-end opening price points in Direct and our move

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away from Gateway-branded consumer electronic products, as well as declines in the Professional segment (\$128 million) primarily due to weaker performance in the business sector and a trend towards large consolidated discounted purchases in the public sector.

Major Product Groups

The following table summarizes our net sales by major product or service group for the past three years (in thousands):

	2006	As %	2005	As %	2004	As %
Desktops	\$1,868,312	46.9%	\$1,894,172	49.2%	\$1,982,141	54.3%
Notebooks	1,437,016	36.1%	1,191,898	30.9%	790,159	21.7%
Servers and other	32,129	0.8%	57,392	1.5%	54,474	1.5%
Total personal computers (PC)	3,337,457	83.8%	3,143,462	81.6%	2,826,774	77.5%
Non-PC	643,346	16.2%	710,599	18.4%	822,960	22.5%
Consolidated net revenues	<u>\$3,980,803</u>		<u>\$3,854,061</u>		<u>\$3,649,734</u>	

Sales of personal computer products represented approximately 84% of total net sales during 2006, as compared to 82% in 2005. As a percentage of total net sales, notebook computer sales increased 5 percentage points during 2006, due to our continued efforts to focus on the notebook computer market and the continued success of our Gateway-branded products in third-party retail. Notebook unit sales increased 48% worldwide compared with a 26% worldwide market unit increase based on the most recent International Data Corporation data.

Sales of non-PC products represented approximately 16% of total net sales during 2006, as compared to 18% in 2005. The decline is primarily due to decreasing unit sales in Direct, which generally yields a higher percentage of non-PC sales than other segments. Non-PC offerings include all products and services other than the PC, including stand-alone displays, peripherals, software, accessories, extended warranty services, training, Internet access, enterprise system, networking products, web portal, and security services. In 2004, we discontinued sales of Gateway branded consumer electronic products.

Net sales of PCs increased in 2004 due to the addition of eMachines PC unit sales subsequent to March 11, 2004 offset by declines in Gateway PC sales due to the closure of the retail stores in April 2004 and lower average selling prices, as well as market share losses in the Professional and Direct segments.

Gross Profit

2006 vs. 2005

Gross profit was \$255 million in 2006 compared with \$322 million in 2005. This decrease in gross profit is largely attributable to lower margins due to competitive pricing pressures in the Retail segment (\$19 million), margin pressure in the Professional segment (\$29 million), and decreased Direct business (\$19 million). As a percentage of net sales, gross profit for 2006 was 6.4%, compared with 8.4% in 2005. Non-PC sales accounted for 73% and 76% of gross profit during 2006 and 2005, respectively.

See "Segment Performance" below for further discussion of gross profit performance on a segment basis.

2005 vs. 2004

Gross profit was \$322 million in 2005 compared with \$307 million in 2004. This increase in gross profit is largely attributable to declines in restructuring, transformation and integration charges (\$86 million) and

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improvements in Retail segment gross profit (\$79 million) based on increased Retail unit volumes and sales revenues, and favorable resolution of a royalty cost dispute (\$6 million), partially offset by gross profit declines in the Direct segment (\$100 million) due to the closure of our Gateway retail stores in April 2004 (\$33 million) and the discontinuation of sale of Gateway-branded consumer electronics, and gross profit declines in the Professional segment (\$50 million) primarily due to price competition. Additionally in 2005, gross profit across all segments was favorably impacted by a change in cost estimate of a certain royalty obligation (\$4 million), offset by the February 2006 Hewlett-Packard agreement related to patent infringement and royalties (\$17 million). As a percentage of net sales, gross profit for 2005 was 8.4% the same amount as 2004. Non-PC sales accounted for approximately 76% and 67% of gross profit during 2005 and 2004, respectively.

Selling, General and Administrative Expenses

2006 vs. 2005

SG&A expenses were \$309 million (including \$0.5 million in restructuring expenses) in 2006 (7.8% of net sales) compared to \$364 million (including \$13 million in restructuring expenses) in 2005 (9.4% of net sales). In addition to the decrease in restructuring expenses (\$13 million), the decrease in SG&A expense is attributable to an increase in 2005 in the sales tax reserve for a tax dispute related to prior years (\$25 million), a 2006 adjustment to the sales tax reserve (\$10 million) due to a favorable settlement from prior year sales tax dispute, decreased headcount-related expenses (\$9.7 million) due to reduced headcount, decreased depreciation expense (\$8.9 million), and other SG&A cost savings (\$3.9 million), partially offset by increases in litigation settlements and professional fees (\$7.8 million) and marketing expense due to increased brand awareness promotions (\$7.7 million).

2005 vs. 2004

SG&A expenses were \$364 million in 2005 (9.4% of net sales) compared to \$909 million in 2004 (24.9% of net sales). The significant decrease in SG&A expense is attributable to a decrease in restructuring, transformation and integration charges (\$379 million), closure of our Gateway retail stores in April 2004 (\$60 million), reduced direct marketing costs partially related to the shift to third-party retail to reduce channel conflict (\$47 million), rationalization of IT expenses (\$32 million), and reductions in corporate overhead, headcount costs and other SG&A cost savings (\$64 million), partially offset by a reserve increase for a sales tax dispute related to prior years (\$25 million) and increased legal spending (\$12 million) during 2005.

Restructuring Activities

We have engaged in several restructuring efforts, including actions related to the closure of our Gateway retail stores, outsourcing of certain processes, workforce reductions and plant closures. We have also incurred costs in connection with certain transformation efforts and our integration with eMachines in 2004. See also Note 13 to the consolidated financial statements. The following table summarizes restructuring, transformation and other charges recorded by Gateway, by income statement classification, for the past three years (in thousands):

	<u>2006</u>	<u>2005</u>	<u>2004</u>
Restructuring:			
Cost of goods sold	\$—	\$ —	\$ 74,735
Selling, general and administrative	<u>479</u>	<u>13,555</u>	<u>336,888</u>
Total	<u>\$479</u>	<u>\$13,555</u>	<u>\$411,623</u>
Transformation and Integration:			
Cost of goods sold	\$—	\$ (86)	\$ 11,251
Selling, general and administrative	<u>—</u>	<u>(411)</u>	<u>54,816</u>
Total	<u>\$—</u>	<u>\$ (497)</u>	<u>\$ 66,067</u>

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During the first quarter of 2004, Gateway adopted a restructuring plan to, among other things, close its remaining 188 retail stores, reduce its workforce, consolidate facilities and outsource certain operating activities. This plan was in addition to previous restructuring plans that were adopted in 2003, 2002 and 2001. All significant restructuring actions are now substantially complete. For all restructuring plans, approximate future cash outflows of \$13 million, primarily lease liabilities on closed facilities, are exceeded by expected future cash inflows of \$15 million from related sublease recoveries and asset dispositions.

Microsoft Agreement

In April 2005, Gateway entered into a Marketing, Development and Settlement Agreement with Microsoft Corporation that provides for Microsoft to make aggregate payments to Gateway of \$150 million (including \$6 million paid directly to our outside legal counsel) on a quarterly basis through the end of 2008. As part of the agreement, Gateway is required to use the remaining \$144 million to fund various marketing and promotional initiatives including advertising, sales training and consulting, as well as the research, development and testing of new Gateway products that run Microsoft products. In 2006 we received and recognized \$34.5 million, compared to \$40.5 million in 2005. Per the agreement, we expect to receive in cash \$8.6 million quarterly through the end of 2008.

Hewlett-Packard Agreement

Following the signing of a binding term sheet in February 2006, Gateway and Hewlett-Packard executed a definitive agreement during the second quarter of 2006, licensing certain portions of their respective patent portfolios to each other. Under the license agreement, Gateway agreed to pay a total of \$47 million, of which Gateway attributed \$16.7 million to resolving, without admission of fault, allegations of past patent infringement, recognizing such cost as a component of cost of goods sold in 2005. The remaining \$30.3 million is attributable to the value of the future seven year cross-licensing agreement.

Operating Income (Loss)

2006 vs. 2005

Operating loss for 2006 totaled \$19 million compared with a loss of \$1 million in 2005. This reflects a decline in gross profit dollars (\$67 million) and benefits related to the April 2005 agreement with Microsoft as discussed in the "Microsoft Agreement" section above (\$6 million), partially offset by an overall focus on SG&A cost savings (\$55 million).

2005 vs. 2004

Operating loss for 2005 totaled \$1 million compared with a loss of \$602 million in 2004. This reflects restructuring, transformation and other special charges discussed in the "Restructuring Activities" section above of \$13 million and \$478 million in 2005 and 2004, respectively. In addition to the significant decline in restructuring, transformation and other special charges, the improvement in 2005 operating income reflects \$40.5 million of benefits related to the April 2005 agreement with Microsoft discussed in the "Microsoft Agreement" section above, as well as the continued positive impact of 2004 initiatives including focus on overall SG&A cost savings, offset by a reserve increase for a prior years sales tax dispute (\$25 million) and the entering into an agreement with Hewlett-Packard in February 2006, related to patent infringement and royalties (\$17 million).

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Other Income, Net

The following table presents the components of other income, net for the periods indicated (in thousands):

	2006	2005	2004
Interest income	\$11,871	\$10,560	\$14,257
Gain (loss) on sales of investments	(195)	1,392	(44)
Gain on extinguishment of liabilities	—	1,229	6,886
Interest expense	(5,720)	(6,116)	(823)
Amortization of debt issuance costs	(1,591)	(1,622)	—
Other, net	(227)	1,348	(29)
Total	<u>\$ 4,138</u>	<u>\$ 6,791</u>	<u>\$20,247</u>

Other income, net includes primarily interest income and expense, and gains and losses of investments, amortization of debt issuance costs and gain from the extinguishment of liabilities. Other income decreased \$3 million in 2006 primarily due to a \$1 million gain on the sale of certain extended service liabilities in the first quarter of 2005 and a \$2 million gain on the sale of a single investment during the second quarter of 2005, partially offset by higher interest income resulting from higher interest rates.

Other income decreased \$13 million in 2005 primarily due to an increase in interest expense, including the amortization of debt issuance costs, as a result of the issuance of \$300 million in senior convertible notes in December 2004 and utilization of the revolving credit facility in 2005, a decrease in interest income and a decrease on gain on extinguishment of liabilities.

Income Taxes

In 2006, we recorded a tax benefit of \$24 million primarily representing a change in tax accrual of \$25 million, together with foreign tax refunds recognized of \$2.1 million, offset by foreign and state tax accruals from operations of \$2.8 million. The change in tax accrual consists primarily of the reversal of previously accrued tax liabilities resulting from various tax authority settlements of \$27 million and recognition of domestic tax refunds of \$6.0 million. The benefit was offset by \$6.2 million of interest accruals relating to previously accrued liabilities, and \$1.5 million of current year accruals established for anticipated tax liabilities. The domestic tax refunds and accrued tax liability reversals represent various settlements between Gateway and the Appeals Office of the Internal Revenue Service with respect to multiple domestic and international issues under audit. These agreements are still subject to review of the Joint Committee on Taxation. We believe the review of the Joint Committee will not adversely impact the recognition of the benefit recorded for these agreements.

In 2005, we recorded a net tax benefit primarily representing the reversal of previously accrued tax liabilities resulting from certain tax authority settlements partially offset by \$1.8 million increase in reserve for a state income and franchise tax dispute. The reversal of the previously accrued tax liabilities represents an agreement between Gateway and the Appeals Office of the Internal Revenue Service with respect to one of the issues under audit. In the fourth quarter of 2005, the benefit recorded from this agreement is \$8.3 million. The agreement is still subject to review of the Joint Committee on Taxation. Gateway believes the review of the Joint Committee will not adversely impact the recognition of the benefit recorded for this agreement.

Segment Performance

Gateway's segment sales and operations are delineated by operating segment as follows:

- **Retail**—includes sales through third-party retail channels of both eMachines and Gateway-branded products;
- **International**—includes international sales and is currently aggregated within the Retail segment for external reporting purposes as it meets the aggregation criteria of SFAS 131, Disclosures about Segments of an Enterprise and Related Information;

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- **Professional**—includes sales to educational institutions (K-12 and higher education), government entities (federal, state and local), small-to-medium businesses, value-added resellers and certain other resellers; and
- **Direct**—includes consumer and small business sales generated via Gateway's web and phone centers as well as legacy revenue streams from Gateway's closed retail stores.

Revenues from these segments are derived from sales of PC and Non-PC products and services. We evaluate segment performance based on sales, gross profit and segment contribution, but do not allocate segment assets or other income and expense items for management reporting purposes. Segment contribution includes selling, general and administrative expenses and other overhead charges directly attributable to the segment and excludes expenses managed outside the reporting segment, including corporate selling, general and administrative expenses, the Microsoft benefit, depreciation and amortization, and the restructuring, transformation and integration charges discussed in "Restructuring Activities" above.

The following table presents key segment performance indicators for the past three years (in thousands):

	2006	Increase (Decrease)	2005	Increase (Decrease)	2004
Net sales:					
Retail (including International)	\$2,739,884	16.2%	\$2,358,669	58.8%	\$1,485,715
Professional	895,774	(9.2)%	986,943	(11.4)%	1,114,493
Direct	345,145	(32.1)%	508,449	(51.6)%	1,049,526
	<u>\$3,980,803</u>	3.3%	<u>\$3,854,061</u>	5.6%	<u>\$3,649,734</u>
Segment gross profit:					
Retail (including International)	\$ 118,050	(13.9)%	\$ 137,076	137.5%	\$ 57,712
Professional	62,189	(32.0)%	91,399	(35.3)%	141,301
Direct	75,122	(20.1)%	93,962	(51.6)%	194,049
	<u>\$ 255,361</u>	(20.8)%	<u>\$ 322,437</u>	(18.0)%	<u>\$ 393,062</u>
Segment contribution:					
Retail (including International)	\$ 96,350	(20.1)%	\$ 120,536	179.3%	\$ 43,161
Professional	(6,509)	(138.4)%	16,937	(71.0)%	58,356
Direct	35,379	(15.0)%	41,601	65.9%	25,070
	<u>\$ 125,220</u>	(30.1)%	<u>\$ 179,074</u>	41.5%	<u>\$ 126,587</u>
Non-segment expenses and other charges	<u>(178,607)</u>	(18.9)%	<u>(220,214)</u>	(69.8)%	<u>(728,565)</u>
Microsoft benefit	34,500	(14.8)%	40,500	100%	—
Consolidated operating loss	<u>\$ (18,887)</u>	(2,851.1)%	<u>\$ (640)</u>	(99.9)%	<u>\$ (601,978)</u>

Retail (including International)

The Retail segment delivered net sales of \$2.7 billion on shipments of 4,171,000 PC units in 2006 as compared with \$2.4 billion on shipments of 3,474,000 PC units in 2005. The increases reflect strong segment performance in the first half of the year due to the continued success of Gateway-branded products in the retail channel as well as growth in our International business. The fourth quarter was negatively impacted by component shortages and softer than normal fourth quarter retail demand in the U.S. and Japan due to Microsoft's launch of its new Vista operating System in January 2007. Channel inventories closed the quarter at unusually low levels as retailers managed down their inventories of Microsoft XP products in anticipation of the January launch of Microsoft Vista.

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Retail segment gross profit was \$118 million (4.3% of sales) in 2006 as compared with \$137 million (5.8% of sales) in 2005. The decline reflects competitive pricing pressures in the second half of the year (\$18 million), higher than expected costs due in part to component price increases (\$17 million), and additional expedited freight and other costs (\$2 million), partially offset by gross profit from increased revenue (\$16 million) and other savings (\$2 million).

Retail segment contribution was \$96 million (3.5% of sales) in 2006 as compared with \$121 million (5.1 % of sales) in 2005. The decline reflects the same factors present in the gross profit discussion above, as well as increased selling, general and administrative expenses (\$5.2 million).

Professional

The Professional segment generated net sales of \$896 million on shipments of 673,000 PC units in 2006 compared with \$987 million on shipments of 749,000 PC units in 2005. The \$91 million decrease in net sales is the result of greater selectivity in contract bidding (\$44 million), declining extended warranty deferred revenue amortization (\$10 million), and competitive pricing (\$37 million).

Professional segment gross profit was \$62 million (6.9% of net sales) in 2006 compared with \$91 million (9.3% of net sales) in 2005. The \$29 million decrease in segment gross profit was attributable to reduced sales volume (\$9 million), declining extended warranty deferred revenue amortization (\$10 million) as stated above, and increases in warranty and royalty expenses (\$10 million).

Professional segment contribution was a loss of \$7 million (0.7% of net sales) in 2006 compared with a \$17 million profit (1.7% of net sales) in 2005. The decline in segment contribution of \$24 million is attributable to the \$29 million decrease in gross profit noted above, partially offset by cost savings from headcount reductions (\$5 million).

Direct

The Direct segment generated net sales of \$345 million on shipments of 169,000 PC units in 2006 compared with \$508 million on shipments of 253,000 PC units in 2005. The decrease in revenue and unit sales is due to a sharp volume decline in telephone based orders (\$134 million), declining extended warranty deferred revenue recognition (\$18 million), and declining Internet access subscription revenue (\$17 million), partially offset by increased average unit prices (\$6 million). The net sales and unit declines were primarily due to marketing that did not drive demand to anticipated levels and our decision at the end of the second quarter of 2006 to shift away from emphasizing products with low opening price points in favor of offering more fully featured solutions. The decline in extended warranty deferred revenue recognition is due to some extended warranty revenue streams reaching full amortization during the year. Similarly, the decline in Internet access subscription revenue is the result of a shrinking subscriber base.

Direct segment gross profit was \$75 million (21.9% of net sales) in 2006 compared with \$94 million (18.5% of net sales) in 2005. The decrease in gross profit of \$19 million is primarily attributable to reduced sales volume.

Direct segment contribution was \$35 million (10.3% of net sales) in 2006 compared to \$42 million (8.2% of net sales) in 2005. The decrease in contribution of \$7 million is attributable to the \$19 million decrease in gross profit noted above partially offset by cost savings in variable sales expenses (\$8 million), headcount reductions (\$2 million), and other expenses (\$2 million).

Non-Segment Expenses

Non-segment expenses and other charges are the costs excluded from our operating segments and primarily consist of general and administrative expenses that are managed on a corporate-wide basis.

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Non-segment expenses and other charges totaled \$179 million in 2006 (including \$0.5 million) in restructuring expenses) as compared with \$220 million in 2005 (including \$13 million in restructuring expenses). The \$41 million decrease consists primarily of changes in the sales tax reserve for a tax dispute related to prior years (\$25 million), a 2006 adjustment to the sales tax reserve (\$10 million) due to a favorable settlement from prior year sales tax dispute, reductions in restructuring expenses (\$13 million), decreased depreciation expense (\$8.2 million), decreased headcount-related expenses (\$1.6 million) due to reduced headcount, and other cost savings (\$1.1 million), partially offset by increases in litigation settlements and professional fees (\$7.8 million), marketing expense (\$6.9 million), and relocation and recruiting costs (\$2.4 million).

Liquidity and Capital Resources

As of December 31, 2006, Gateway had approximately \$416 million in cash and marketable securities as compared with \$586 million at the end of 2005.

The following table presents selected financial statistics and information related to cash as of December 31 for the periods indicated (dollars in thousands):

	For each of the quarters ending December 31		
	2006	2005	2004
Cash and marketable securities	\$ 416,335	\$ 585,688	\$ 588,330
Days of sales in accounts receivable (a)	25	28	30
Days inventory on hand (b)	9	19	19
Days in accounts payable (c)	(58)	(67)	(51)
Cash conversion cycle before days in supplier receivables	(24)	(20)	(2)
Days in supplier receivables (d)	23	19	8
Cash conversion cycle (e)	(1)	(1)	6

- Days of sales in accounts receivable measures the average number of days receivables are outstanding and is calculated by dividing accounts receivable (net of allowances for doubtful accounts) by the most recent quarterly net sales divided by the number of days in the quarter.
- Days inventory on hand measures the average number of days of inventory from product procurement to sale and is calculated by dividing inventory by the most recent quarterly cost of goods sold divided by the number of days in the quarter.
- Days in accounts payable measures the average number of days our accounts payable balances are outstanding and is calculated by dividing accounts payable by the most recent quarterly cost of goods sold divided by the number of days in the quarter.
- Gateway purchases selected components from suppliers and, where possible, in lieu of a consignment arrangement, resells the components to original design manufacturers to incorporate into products being manufactured for Gateway. The receivable from the sale of the components to the original design manufacturer is recorded in "Receivables from suppliers". Supplier receivables amounted to \$247 million, \$214 million, and \$79 million at December 31, 2006, 2005, and 2004, respectively. Days in supplier receivables measures the average number of days supplier receivables are outstanding and is calculated by dividing supplier receivables by the most recent quarterly cost of goods sold divided by the number of days in the quarter. The increase in days in receivables from suppliers in 2006 is due to the inclusion of three additional original design manufacturers in Gateway's buy-sell program.
- The cash conversion cycle is the sum of days in accounts receivable and inventory on hand and in supplier receivables less days in accounts payable and effectively measures the number of days from component purchases to cash collection on customer sales.

We used \$69 million in cash in support of operating activities in 2006. Significant factors affecting cash used in operations included net income adjusted for non-cash items of \$48 million, and a net decrease in accounts

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receivable and inventory of \$190 million offset by an increase in other assets of \$72 million, and a net decrease in accounts payable, accrued liabilities, accrued royalties and other liabilities of \$236 million. The decrease in accounts receivable was due to lower sales activity in the fourth quarter of 2006 as compared to the fourth quarter of 2005 and an increased focus by management to reduce aged accounts receivables. The decrease in inventory was driven primarily by management's focus on reducing remanufactured units held for sale and "in-transit" finished goods, while Other Assets increased primarily due to increased Receivable from suppliers. Accounts payable decreased in connection with management's desire to improve relations with its key vendors by shortening its days in accounts payable. Accrued Liabilities and Royalties decreased due to reduced sales activity in fourth quarter 2006 as compared to the fourth quarter 2005. Other Liabilities decreased due to a reduction of deferred revenue. We used approximately \$55 million in cash for capital expenditures primarily for the development of our new ERP system and \$128 million to purchase marketable securities, offset by proceeds from sales of marketable securities of \$222 million. From a financing perspective, we paid \$50 million on our line of credit.

We used \$25 million in cash in support of operating activities in 2005. Significant factors affecting cash used in operations included a net increase in accounts receivable, inventory and other assets of \$238 million, offset by a net income adjusted for non-cash items of \$83 million, and a net increase in accounts payable, accrued expenses and other liabilities of \$130 million. The increase in accounts receivable was driven by an increased mix of Retail sales. The increase in inventory was driven primarily by the increased level of finished products for Retail as well as an increase in component inventories, while accounts payable increased in connection with new supply and manufacturing agreements. The increase in days in accounts payable of 16 days from 2004 to 2005 was due to changed supplier terms and conditions. Other assets increased due to the increased sale of components to original design manufacturers to incorporate into products being manufactured for us. We used approximately \$40 million in cash for capital expenditures and \$45 million to purchase marketable securities, offset by proceeds from sales of marketable securities of \$190 million.

We used \$434 million in cash in support of operations during 2004, including \$271 million of net loss adjusted for non-cash items. Other significant factors affecting cash used in operations include a net increase in accounts receivable of \$59 million (after giving effect for the \$120 million in accounts receivable assumed through acquisition of eMachines) due to the shift in our business model from our former retail stores to third party retail and decreases in current and other liabilities of \$209 million (including settlement of most of the \$277 million in current liabilities assumed in connection with the eMachines' acquisition), partially offset by declines in inventory and other assets of \$104 million (after giving effect for the \$153 million in inventory and other assets assumed through acquisition of eMachines). From an investing perspective, we generated proceeds of approximately \$485 million through the liquidation of marketable securities and the sale of an idled facility and used \$41 million in acquisition of eMachines, \$22 million to settle a shareholder note payable and approximately \$35 million in acquisition of capital assets. From a financing perspective, we generated a net \$291 million through a \$300 million convertible debt offering, \$50 million through borrowings against our credit facility, and \$12 million through employee stock option exercises while using \$280 million to purchase treasury stock and redeem the Series A and C Preferred Stock held by AOL and \$9 million to pay preferred stock dividends.

Our cash position varies during any particular period, but historically increases at quarter-end due to additional focus by management on accounts receivable, inventory, accounts payable and credit facility balances. Although our quarter-end cash balance is one analytical measure used by our suppliers in evaluating credit terms, we believe our payment performance is a more important factor to our suppliers. Accordingly, over the past few quarters we have reduced our days in accounts payable as part of an overall strategy to improve our supplier relations. We also lowered our credit facility borrowings by \$50 million during 2006.

Looking to 2007 our goal is to reverse the negative cash flows from operations through improving our overall financial results by improving product sales and gross profit, reducing SG&A costs, improving management of working capital, and aggressively defending litigation matters to minimize or avoid settlement charges. However, we can give no assurance that we will be successful in achieving any of these goals.

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We believe that our sources of capital will be sufficient to fund anticipated working capital requirements, restructuring actions, capital expenditures and cash required for other activities for at least the next twelve months. However, cash flows from future operations and investing activities and the precise amount and timing of our future financing needs are uncertain. Future cash flow will depend on a number of factors, including our ability to achieve the goals set forth in the preceding paragraph, and those factors set forth in Item 1A—Risk Factors. Should we be unable to meet our cash needs from our current sources of capital, we would most likely incur additional restructuring charges to adjust our expenditures to a level that our cash flows could support and/or seek financing from other sources including additional equity offerings. Given our history of sales declines and losses, there is no assurance that, if needed, we would be able to obtain financing from external sources, or maintain current credit lines with vendors.

Debt

In October 2004, we entered into a credit agreement with a major financial institution that provides for a borrowing base under a revolving credit facility of up to \$200 million. Our borrowing base fluctuates primarily as a function of our outstanding accounts receivable. Borrowings under this agreement bear interest at variable-term LIBOR or prime rates, at our election. As of December 31, 2006 and December 31, 2005, we had \$0 and \$50 million, respectively in borrowings outstanding under this agreement. The interest rate as of December 31, 2006 was 7.25%. This interest rate adjusts with changes in the prime rate. We also utilized the credit agreement to support \$36 million of stand-by letters of credit and had borrowing availability of \$35 million. In addition to usual and customary covenants for an arrangement of its type, the credit agreement includes certain financial covenants. Gateway renegotiated the credit agreement as of December 26, 2006 to replace the financial covenant that we maintain a certified cash balance of \$150 million with covenants that we maintain a liquidity position of \$100 million and negative cash flow not to exceed \$40 million and \$57 million for the fourth quarter of 2006 and the first quarter of 2007, respectively, and \$60 million for each quarter thereafter, with cumulative negative cash flow not to exceed \$120 million. Further, once we have achieved 3 consecutive quarters of positive excess cash flow, the amended credit agreement requires that we maintain positive cash flow in each quarter thereafter. The agreement expires on October 31, 2010, at which time all amounts then outstanding will be due and payable.

In December 2004, we completed the sale of \$300 million of senior convertible notes through a private placement to institutional investors, including \$150 million at 1.5% per year due December 31, 2009 and \$150 million at 2.0% per year due December 2011. Additional information regarding our convertible debt can be found in Note 3 to the Consolidated Financial Statements.

Restructuring Obligations

During the first quarter of 2004, Gateway adopted a restructuring plan to, among other things, close its remaining 188 retail stores, reduce its workforce, consolidate facilities and outsource certain operating activities. This plan was in addition to previous restructuring plans that were adopted in 2003, 2002 and 2001. All significant restructuring actions are now substantially complete. For all restructuring plans, approximate future cash outflows of \$13 million, primarily lease liabilities on closed facilities, are exceeded by expected future cash inflows of \$15 million from related sublease recoveries and asset dispositions. These amounts are included in the Operating lease category in the Contractual Obligations table below. See also Note 13 to the Consolidated Financial Statements.

We believe that our current sources of working capital provide adequate flexibility for our financial needs for at least the next twelve months. However, any projections of future financial needs and sources of working capital are subject to uncertainty. See “Forward Looking Statements” and Item 1A “Risk Factors” for events that could affect our estimates of future financial needs and sources of working capital.

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Contractual Obligations

The cash impact of our contractual obligations associated with operating leases, royalty and licensing agreements, purchase obligations and announced restructurings is as follows:

	Payments due by Period (in thousands)				
	Total	Less than 1 Year	2-3 Years	4-5 Years	More than 5 Years
Operating leases (1)	\$ 14,904	\$ 7,659	\$ 12,645	\$ 1,739	\$ (7,139)
Royalty/Licensing agreements (2)	34,710	25,525	5,652	3,533	—
Debt, including estimated interest obligations	321,750	5,250	160,500	156,000	—
Estimated purchase obligations (3)	107,270	107,270	—	—	—
Total	<u>\$478,634</u>	<u>\$145,704</u>	<u>\$178,797</u>	<u>\$161,272</u>	<u>\$ (7,139)</u>

- (1) Represents lease obligations, net of anticipated sublease cash receipts, including amounts that have been accrued in connection with certain restructuring actions. See Notes 5 and 13 to the Consolidated Financial Statements for additional information.
- (2) Includes \$22 million payment due to Hewlett-Packard pursuant to the cross-licensing agreement.
- (3) Purchase obligations include agreements to purchase goods or services (such as minimum levels of outsourced support services) that are enforceable, legally binding and specify all significant terms, including: the quantity to be purchased, the price to be paid and the timing of the purchase. These figures exclude agreements or amounts that are cancelable without penalty. The materials purchase obligation portion of this amount represents approximately six weeks of supply in our manufacturing channel.

Off-Balance Sheet Arrangements and Other

We do not participate in transactions that generate relationships with unconsolidated entities or financial partnerships, such as special purpose entities ("SPEs") or variable interest entities ("VIEs"), which would have been established for the purpose of facilitating off-balance sheet arrangements or other limited purposes.

During the normal course of business, we make certain indemnities, commitments and guarantees under which we may be required to make payments in relation to certain transactions. These include: (i) intellectual property indemnities to our customers and licensees in connection with the use, sales and/or license of our products, (ii) indemnities to vendors and service providers pertaining to claims based on the negligence or willful misconduct of Gateway and (iii) indemnities involving the accuracy of representations and warranties in certain contracts. In addition, we have made contractual commitments to several employees providing for payments upon the occurrence of certain prescribed events. The majority of these indemnities, commitments and guarantees do not provide for any limitation of the maximum potential for future payments Gateway could be obligated to make. We have not recorded any liability for these indemnities, commitments and other guarantees in the accompanying consolidated balance sheets.

New Accounting Pronouncements

See Note 1 to the Consolidated Financial Statements in Item 8 for a full description of recent accounting pronouncements, including the expected dates of adoption and estimated effects on results of operations and financial position, which is incorporated herein by reference.

Subsequent Event

On February 13, 2007, Gateway received notification from Revenue Ireland, the Irish taxing authority, that it had waived all further consideration related to possible capital gains treatment resulting from the dissolution and liquidation of certain Gateway entities in Europe. These entities ceased operations in 2001 and have been in the process of liquidation since then. Based on this notification, Gateway reduced its income taxes payable and increased the related income tax benefit as of and for the year ended December 31, 2006 by \$2.7 million.

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Item 7A. *Quantitative and Qualitative Disclosures About Market Risk*

We are generally not subject to material market risk with respect to our investments classified as marketable securities as such investments are readily marketable, liquid and do not fluctuate substantially from stated value. Regarding long-term investments, Gateway holds and may continue to consider investments in minority interests in companies having operations or technology in areas within Gateway's strategic focus. Adverse changes in market conditions such as occurred in the years starting in 2000, and poor operating results of certain of these underlying investments, have resulted and may in the future result in Gateway incurring losses or an inability to recover the original carrying value of our investments. As of December 31, 2006, we held long term investments of approximately \$3 million.

In October 2004, Gateway entered into a credit agreement with a major financial institution to provide for a revolving credit facility of up to an aggregate of \$200 million. Borrowings under this agreement bear interest at variable-term LIBOR or prime rates, at Gateway's election. As of December 31, 2006 and December 31, 2005, Gateway had \$0 and \$50 million, respectively in borrowings outstanding under this agreement. The interest rate as of December 31, 2006 was 7.25%. This interest rate adjusts with changes in the prime rate. We also utilized the credit agreement to support \$36 million of stand-by letters-of credit and had borrowing availability of \$35 million.

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Item 8. Consolidated Financial Statements and Supplementary Data

INDEX TO CONSOLIDATED FINANCIAL STATEMENTS AND FINANCIAL STATEMENT SCHEDULE

Financial Statements:

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<u>Consolidated Statements of Cash Flows for the Years Ended December 31, 2006, 2005, and 2004</u>	43
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Report of Independent Registered Public Accounting Firm

To the Board of Directors and Stockholders of Gateway, Inc.

We have audited the accompanying consolidated balance sheets of Gateway, Inc. and subsidiaries ("the Company") as of December 31, 2006 and 2005, and the related consolidated statements of operations, cash flows, and stockholders' equity for each of the three years ended December 31, 2006. Our audit also included the accompanying financial statement schedule for the years ended December 31, 2006, 2005, and 2004. These financial statements and the financial statement schedule are the responsibility of the Company's management. Our responsibility is to express an opinion on these financial statements and financial statement schedule based on our audits.

We conducted our audits in accordance with standards of the Public Company Accounting Oversight Board (United States). Those standards require that we plan and perform the audit to obtain reasonable assurance about whether the financial statements are free of material misstatement. An audit includes examining, on a test basis, evidence supporting the amounts and disclosures in the financial statements. An audit also includes assessing the accounting principles used and significant estimates made by management, as well as evaluating the overall financial statement presentation. We believe that our audits provide a reasonable basis for our opinion.

In our opinion, such consolidated financial statements present fairly, in all material respects, the financial position of Gateway, Inc. and subsidiaries as of December 31, 2006 and 2005, and the results of their operations and their cash flows for each of the three years ended December 31, 2006 in conformity with accounting principles generally accepted in the United States of America. Also, in our opinion, such financial statement schedule, when considered in relation to the basic consolidated financial statements taken as a whole, presents fairly, in all material respects, the information set forth therein.

As discussed in Note 8 to the consolidated financial statements, the Company changed its method of accounting for share-based payments to conform to Statement of Financial Accounting Standards No. 123(R), Share-based Payment, as of January 1, 2006.

We have also audited, in accordance with the standards of the Public Company Accounting Oversight Board (United States), the effectiveness of the Company's internal control over financial reporting as of December 31, 2006, based on the criteria established in *Internal Control—Integrated Framework* issued by the Committee of Sponsoring Organizations of the Treadway Commission and our report dated February 23, 2007 expressed an unqualified opinion on management's assessment of the effectiveness of the Company's internal control over financial reporting and an adverse opinion on the effectiveness of the Company's internal control over financial reporting.

/s/ DELOITTE & TOUCHE LLP

Costa Mesa, California
February 23, 2007

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GATEWAY, INC.
CONSOLIDATED STATEMENTS OF OPERATIONS
For the years ended December 31, 2006, 2005 and 2004
(in thousands, except per share amounts)

	2006	2005	2004
Net sales	\$3,980,803	\$3,854,061	\$3,649,734
Cost of goods sold	<u>3,725,442</u>	<u>3,531,623</u>	<u>3,342,662</u>
Gross profit	255,361	322,438	307,072
Selling, general and administrative expenses	308,738	363,578	909,050
Microsoft benefit	<u>34,500</u>	<u>40,500</u>	<u>—</u>
Operating loss	(18,877)	(640)	(601,978)
Other income, net	4,138	6,791	20,247
Minority interest	<u>(18)</u>	<u>—</u>	<u>—</u>
Income (loss) before income taxes	(14,757)	6,151	(581,731)
Income tax benefit	<u>24,400</u>	<u>10</u>	<u>14,113</u>
Net income (loss)	9,643	6,161	(567,618)
Preferred stock dividends and accretion	—	—	(7,991)
Gain on redemption of preferred stock	—	—	100,133
Net income (loss) attributable to common stockholders	<u>\$ 9,643</u>	<u>\$ 6,161</u>	<u>\$ (475,476)</u>
Net income (loss) per common share:			
Basic	<u>\$ 0.03</u>	<u>\$ 0.02</u>	<u>\$ (1.31)</u>
Diluted (Note 1)	<u>\$ 0.03</u>	<u>\$ 0.02</u>	<u>\$ (1.45)</u>
Weighted average shares outstanding:			
Basic	<u>373,001</u>	<u>371,661</u>	<u>363,708</u>
Diluted (Note 1)	<u>374,023</u>	<u>372,167</u>	<u>391,115</u>

The accompanying notes are an integral part of the consolidated financial statements.

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GATEWAY, INC.
CONSOLIDATED BALANCE SHEETS
December 31, 2006 and 2005
(in thousands, except per share amounts)

	2006	2005
ASSETS		
Current assets:		
Cash and cash equivalents	\$ 345,677	\$ 422,488
Marketable securities	70,658	163,200
Accounts receivable, net of allowance for uncollectible accounts of \$2,218 and \$6,092 at December 31, 2006 and 2005, respectively	274,782	345,288
Inventory:		
Components and subassemblies	18,181	71,163
Finished goods	79,006	148,181
Total inventory	97,187	219,344
Receivables from suppliers	247,207	213,901
Other	215,582	209,851
Total current assets	1,251,093	1,574,072
Property, plant and equipment, at cost	341,576	484,535
Less: Accumulated depreciation and amortization	(230,645)	(401,379)
Property, plant and equipment, net	110,931	83,156
Intangible assets, at cost	129,277	99,000
Less: Accumulated amortization	(67,377)	(59,538)
Intangible assets, net	61,900	39,462
Goodwill and non-amortizable intangible assets	205,219	205,219
Restricted cash	3,266	3,754
Long-term investments	3,159	3,159
Deferred debt issue costs	6,010	7,600
Other assets, net	14,657	4,643
	<u>\$1,656,235</u>	<u>\$1,921,065</u>
LIABILITIES AND STOCKHOLDERS' EQUITY		
Current liabilities:		
Revolving credit facility	\$ —	\$ 50,000
Accounts payable	612,639	761,895
Accrued expenses	159,199	178,066
Warranty	46,616	34,615
Restructuring	13,046	25,897
Other accrued liabilities	11,254	10,533
Accrued royalties	54,521	68,216
Deferred revenue	27,701	57,834
Income taxes payable	91,213	113,918
Other current liabilities	2,745	3,993
Total current liabilities	1,018,934	1,304,967
Senior convertible notes	300,000	300,000
Deferred revenue	14,895	33,226
Warranty	18,223	2,425
Deferred tax liabilities	19,840	19,840
Other long-term liabilities	12,917	5,334
Total liabilities	1,384,809	1,665,792
Minority interest	2,418	—
Commitments and contingencies (Note 5)		
Stockholders' equity:		
Common stock, \$.01 par value, 1,000,000 shares authorized; 376,989 and 377,239 shares issued in 2006 and 2005, respectively	3,770	3,773
Additional paid-in capital	973,895	971,761
Common stock in treasury, at cost, 5,347 and 4,061 shares for 2006 and 2005, respectively	(26,448)	(23,253)
Deferred stock-based compensation	(2,746)	(6,352)
Accumulated deficit	(678,243)	(687,886)
Accumulated other comprehensive loss	(1,220)	(2,770)
Net stockholders' equity	269,008	255,273
	<u>\$1,656,235</u>	<u>\$1,921,065</u>

The accompanying notes are an integral part of the consolidated financial statements.

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GATEWAY, INC
CONSOLIDATED STATEMENTS OF CASH FLOWS
For the years ended December 31, 2006, 2005, and 2004
(in thousands)

	2006	2005	2004
Cash flows from operating activities:			
Net income (loss)	\$ 9,643	\$ 6,161	\$(567,618)
Adjustments to reconcile net income (loss) to net cash provided by (used in) operating activities:			
Write-down of long-lived assets	1,270	16,101	156,710
Depreciation and amortization	27,578	38,816	112,225
Provision for doubtful accounts receivable	2,540	5,529	11,198
Stock-based compensation	5,732	13,663	13,617
Loss on sales of investments	118	519	46
(Gain) loss on sale of property, plant and equipment	(23)	—	2,500
Other, net	1,591	1,874	643
Changes in operating assets and liabilities, net of the effects of the eMachines' acquisition:			
Accounts receivable	67,966	(8,696)	(59,316)
Inventory	122,157	(23,020)	63,512
Other assets	(72,197)	(205,825)	40,793
Accounts payable	(152,067)	222,595	(94,685)
Accrued expenses	(23,472)	(24,721)	(32,284)
Accrued royalties	(13,695)	26,420	(19,289)
Other liabilities	(46,616)	(94,143)	(62,250)
Net cash used in operating activities	(69,475)	(24,727)	(434,198)
Cash flows from investing activities:			
Purchases of available-for-sale securities	(127,813)	(44,993)	(113,199)
Sales of available-for-sale securities	221,683	189,874	586,176
Purchases of property, plant and equipment	(55,435)	(40,427)	(34,467)
Proceeds from sale of property, plant and equipment	4,504	13,875	12,086
Cash paid in acquisition of eMachines, net of cash acquired	—	—	(41,350)
Payment of shareholder note payable	—	—	(22,448)
Net cash provided by investing activities	42,939	118,329	386,798
Cash flows from financing activities:			
Payment of preferred dividends	—	—	(8,840)
Proceeds from stock option exercises	5	1,093	11,668
Proceeds from the issuance of senior convertible notes, net	—	—	290,862
Proceeds from revolving credit facility	—	—	50,000
Payment from revolving credit facility	(50,000)	—	—
Purchase of Series A and C preferred stock	—	—	(264,253)
Purchase of treasury stock	(280)	—	(15,764)
Net cash provided by (used in) financing activities	(50,275)	1,093	63,673
Net increase (decrease) in cash and cash equivalents	(76,811)	94,695	16,273
Cash and cash equivalents, beginning of year	422,488	327,793	311,520
Cash and cash equivalents, end of year	\$ 345,677	\$ 422,488	\$ 327,793
Supplemental disclosure of cash flow information:			
Cash paid during the period for interest	\$ 6,533	\$ 6,858	\$ 476
Cash received during the period for income taxes	\$ 3,957	\$ 2,257	\$ 2,144
Supplemental disclosure of non cash investing and financing activities:			
Minority interest in earnings	\$ 18	\$ —	\$ —
Value of common stock issued in acquisition of eMachines	\$ —	\$ —	\$ 214,623
Accretion of Series C preferred stock	\$ —	\$ —	\$ 2,280
Value of restricted shares withheld for taxes	\$ 3,195	\$ 7,489	\$ —

Preferred stock surrendered in payment of receivable due from AOL \$ — \$ — \$ 35,614

The accompanying notes are an integral part of the consolidated financial statements.

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GATEWAY, INC.
CONSOLIDATED STATEMENTS OF CHANGES IN STOCKHOLDERS' EQUITY
For the years ended December 31, 2006, 2005, and 2004
(in thousands)

	Series A Preferred Stock		Common Stock		Treasury Stock		Additional Paid-In Capital	Deferred Stock- Based Compensation	Retained Earnings (Accumulated Deficit)	Accumulated Other Comprehensive Income (Loss)	Net Equity
	Shares	Amount	Shares	Amount	Shares	Amount	Amount	Amount	Amount	Amount	Amount
Balance, January 1, 2004	50	\$ 200,000	324,392	\$ 3,244	—	\$ —	\$ 734,550	\$ —	\$ (218,571)	\$ 2,795	\$ 722,018
Net loss									(567,618)		(567,618)
Foreign currency translation										(1,643)	(1,643)
Net unrealized loss on available for sale securities, net of tax										(728)	(728)
Total comprehensive loss											(569,989)
Issuance of stock in acquisition of eMachines			42,281	423			190,266				190,689
Issuance of restricted stock in acquisition of eMachines			5,307	53			27,491	(27,544)			—
Issuance of stock through option exercises, including tax benefit of \$ 656			2,959	29			12,295				12,324
Redemption of Series A preferred stock	(50)	(200,000)									(200,000)
Acquisition of treasury stock					2,725	(15,764)					(15,764)
Gain on redemption of Series A and C preferred stock									100,133		100,133
Dividends declared and accretion of redeemable preferred stock									(7,991)		(7,991)
Compensation expense on stock options and restricted stock							512	13,105			13,617
Balance, December 31, 2004	—	\$ —	374,941	\$ 3,749	2,725	\$ (15,764)	\$ 965,114	\$ (14,439)	\$ (694,047)	\$ 424	\$ 245,037
Net income									6,161		6,161
Foreign currency translation										517	517
Net unrealized loss on available for sale securities, net of tax										(3,711)	(3,711)
Total comprehensive income											2,967
Cancellations of restricted stock			(99)	(1)			(237)	238			—
Issuance of stock, including tax benefit of \$ 227			2,397	25			6,884	(5,589)			1,320
Acquisition of treasury stock					1,336	(7,489)					(7,489)
Compensation											

expense on stock options and restricted stock								13,438			13,438
Balance, December 31, 2005	<u>—</u>	<u>\$ —</u>	<u>377,239</u>	<u>\$ 3,773</u>	<u>4,061</u>	<u>\$(23,253)</u>	<u>\$ 971,761</u>	<u>\$ (6,352)</u>	<u>\$ (687,886)</u>	<u>\$ (2,770)</u>	<u>\$ 255,273</u>
Net income									9,643		9,643
Foreign currency translation										104	104
Net unrealized loss on available for sale securities, net of tax										1,446	1,446
Total comprehensive income											11,193
Cancellations of restricted stock			(583)	(6)			(1,667)	1,673			—
Issuance of stock, including tax benefit of \$ 313			333	3			668	(353)			318
Acquisition of treasury stock					1,286	(3,195)					(3,195)
Compensation expense on stock options and restricted stock							3,133	2,286			5,419
Balance, December 31, 2006	<u>—</u>	<u>\$ —</u>	<u>376,989</u>	<u>\$ 3,770</u>	<u>5,347</u>	<u>\$(26,448)</u>	<u>\$ 973,895</u>	<u>\$ (2,746)</u>	<u>\$ (678,243)</u>	<u>\$ (1,220)</u>	<u>\$ 269,008</u>

The accompanying notes are an integral part of the consolidated financial statements.

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GATEWAY, INC.

NOTES TO CONSOLIDATED FINANCIAL STATEMENTS

1. Nature of Operations and Summary of Significant Accounting Policies:

Gateway directly and indirectly sells its desktop and notebook computers and servers ("PCs"), PC-related products and services that are enabled by or connect with PCs to third-party retailers, consumers, businesses, government agencies and educational institutions. PC-related products and services ("Non-PC") consist of all products and services other than the PC, including stand-alone displays, peripherals, software, accessories, extended warranty services, training, Internet access, web portals, security services, enterprise system and networking products and services.

On March 11, 2004, Gateway completed its acquisition of eMachines, Inc., a privately-held computer company. These consolidated financial statements include eMachines' results of operations subsequent to March 11, 2004 (see Note 10).

During 2006, Gateway entered into a joint venture agreement with a significant original design manufacturer to provide a dedicated U.S. final assembly facility in La Vergne, Tennessee. Beginning in June 2006 and continuing through October 2006, Gateway invested \$5.6 million in this joint venture, known as Gateway Pro Partners, LLC ("GCC"). Gateway holds the majority ownership interest in GCC and accounts for this entity as a consolidated subsidiary. GCC assembles configure-to-order desktops, notebooks and servers according to Gateway customer specifications. GCC also provides custom imaging services and government compliance certification.

The significant accounting policies used in the preparation of the consolidated financial statements of Gateway are as follows:

(a) Basis of Presentation:

The consolidated financial statements include the accounts of Gateway and its subsidiaries. All intercompany accounts and transactions have been eliminated in consolidation. Gateway records minority interest expense related to its consolidated subsidiaries which are not wholly owned.

(b) Use of Estimates:

The preparation of financial statements in conformity with accounting principles generally accepted in the United States of America requires management to make estimates and assumptions that affect the reported amounts of assets and liabilities and the disclosure of contingent assets and liabilities at the date of the financial statements and the reported amounts of revenue and expenses during the reporting period. Actual results could differ from those estimates. Significant estimates include the fair values ascribed to severable contract elements, provisions for sales returns, bad debts in accounts receivable, excess and/or obsolete inventory, product warranty costs, customer incentive programs including rebates, employee incentive programs including bonus and options, restructuring activities, deferred tax assets, and litigation matters.

(c) Cash and Cash Equivalents:

Gateway considers all highly liquid investments with original maturities of three months or less to be cash equivalents. The carrying amount of these investments approximates fair value because of their short maturities.

(d) Marketable Securities:

Marketable securities consist of investments in commercial paper, debt securities, mutual funds, and equity securities with readily determinable fair values and are classified as available for sale and carried at fair market value based on quoted market prices. Unrealized gains and losses are recorded as a component of accumulated

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GATEWAY, INC.

NOTES TO CONSOLIDATED FINANCIAL STATEMENTS—(Continued)

other comprehensive loss. The specific identification method is used to determine the cost basis in computing realized gains or losses on dispositions of marketable securities.

Gateway regularly monitors and evaluates the realizable value of its investments. When assessing investments for other-than-temporary declines in value, Gateway considers such factors as, among other things, how significant the decline in value is as a percentage of the original cost, how long the market value of the investment has been below original cost, Gateway's ability and intent to continue holding the investment. If events and circumstances indicate that an other-than-temporary decline in the value of an investment has occurred, Gateway records an impairment charge to income in that period.

Included in marketable securities as of December 31, 2006 and 2005 are unrealized losses of approximately \$0.3 million and \$1.7 million, respectively. No single security's unrealized loss position is considered significant as a percentage of its cost and management believes Gateway has the ability and intent to hold the underlying securities to maturity and for this reason; no other-than-temporary impairment charge was recorded during either 2006 or 2005.

(e) Inventory:

Inventory, which is comprised of component parts, both owned and consigned, subassemblies and finished goods, including refurbished PCs, is valued at the lower of weighted average cost or market. Component parts and subassemblies consist of raw materials and products other than the PC such as stand-alone displays, peripherals, software not included with the PC, and accessories. Gateway performs an assessment of its inventories quarterly, reviewing the amounts of inventory on hand and under commitment against its latest forecasted demand requirements to determine whether excess or obsolescence write-downs are required.

Inventory-in-transit balances were approximately \$9 million and \$67 million as of December 31, 2006 and 2005, respectively.

(f) Receivables from Suppliers:

Gateway purchases selected components from suppliers and resells the components to original design manufacturers to incorporate into products being manufactured for Gateway. The receivable from these sales of the components is recorded as "Receivables from suppliers". If substantial uncertainty regarding the collectibility of these receivables is noted, an appropriate reserve may be required, which would affect earnings in the period the uncertainty is identified. As of December 31, 2006 and 2005, reserve balances were \$0.

(g) Internal-use Software:

Gateway capitalizes only those direct costs associated with the actual development or acquisition of computer software for internal use, including costs associated with the design, coding, installation and testing of the system. Costs associated with preliminary development, such as the evaluation and selection of alternatives, as well as training, maintenance and support are expensed as incurred. Gateway is currently migrating to a new enterprise resource planning system as well as new order-capture and back-end service and support systems. A significant change to the planned use of internal-use software could result in a material impairment charge in the reporting period that the change was made.

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GATEWAY, INC.

NOTES TO CONSOLIDATED FINANCIAL STATEMENTS—(Continued)

(h) Property, Plant and Equipment:

Property, plant and equipment are stated at cost. Depreciation is provided using the straight-line method over the assets' estimated useful lives, as follows:

	<u>Estimated Useful Life (Years)</u>
Office and Production Equipment	1-7
Furniture and Fixtures	7-10
Internal-use Software	3-7
Vehicles	3
Leasehold Improvements	Lesser of 10 or Lease Life
Buildings	35

Upon sale or retirement of property, plant and equipment, the related costs and accumulated depreciation or amortization are removed from the accounts and any gain or loss is included in the determination of net income (loss).

As part of Gateway's 2003 and 2004 restructuring efforts, the estimated useful lives of certain assets were shortened. These revisions to estimated useful lives resulted in additional depreciation expense of \$0, \$5 million (\$.01 per share), and \$31 million (\$.08 per share) for 2006, 2005, and 2004, respectively.

(i) Intangible Assets and Goodwill:

Intangible assets with finite lives are amortized on a straight-line basis over their estimated useful lives, generally four to ten years. Intangible assets with indefinite lives such as trade names and goodwill are not amortized. Intangible assets are reviewed for impairment whenever events or circumstances indicate an event of impairment may exist. During 2004, Gateway revised the estimated useful lives of certain intangible assets based on planned changes in the asset's use, resulting in additional amortization expense of \$0, \$1.1 million and \$3.3 million in 2006, 2005 and 2004, respectively (see Note 13). Non-amortizable intangible assets, including goodwill, are reviewed for impairment annually during the fourth quarter (based on a discounted cash flow model under the income approach) or whenever events or circumstances indicate an event of impairment may exist. Management's fourth quarter 2006 analysis concluded that no condition of non-amortizable intangible asset impairment existed as of December 31, 2006.

Intangible assets with finite lives acquired through the acquisition of eMachines, including customer-related assets, were assigned useful lives of ten years. Amortization expense related to these assets approximates \$4.8 million annually.

Total intangible asset amortization expense was \$7.8 million, \$6.3 million (including \$1.1 million in accelerated amortization), and \$16.6 million (including \$3.3 million in accelerated amortization) for 2006, 2005, and 2004, respectively.

(j) Long-lived Assets:

Gateway reviews long-lived assets for impairment whenever events or changes in circumstances indicate that the carrying amount of an asset may not be recoverable. An asset is considered to be impaired when the sum of the undiscounted net future cash flows expected to result from the use of the asset and its eventual disposition does not exceed its carrying amount. The amount of impairment loss, if any, is measured as the difference between the net book value of the asset and its estimated fair value based on appraised or other estimated values. For the years ending December 31, 2006, 2005 and 2004, Gateway recorded \$1.3 million, \$20 million, and \$162 million for impairment of long-lived assets, respectively.

Table of Contents**GATEWAY, INC.****NOTES TO CONSOLIDATED FINANCIAL STATEMENTS—(Continued)****(k) Royalties:**

Gateway has royalty-bearing license agreements that allow Gateway to sell certain hardware and software which are protected by patent, copyright or license. Royalty costs are accrued and included in cost of goods sold when products are shipped or amortized over the period of benefit when the license terms are not specifically related to the units shipped.

(l) Warranty:

Gateway provides standard warranties with the sale of its products. The estimated cost of providing the product warranty is recorded at the time revenue is recognized. Gateway maintains product quality programs and processes including monitoring and evaluating the quality of its suppliers. Estimated warranty costs are affected by ongoing product failure rates, specific product class failures outside of experience and material usage and service delivery costs incurred in correcting a product failure or in providing customer support. A summary of changes in Gateway's accrued warranty liability, which is included in both current liabilities and non-current liabilities, is as follows (in thousands):

	2006	2005
Accrued warranty, beginning of the year	\$ 37,040	\$ 19,291
Accruals for warranties issued during the year	80,697	58,746
Change in management estimate	12,000	—
Settlements made	(64,898)	(40,997)
Accrued warranty, end of the year	<u>\$ 64,839</u>	<u>\$ 37,040</u>

(m) Trade Payables Program:

During 2005 and 2006, Gateway had an accelerated supplier payment program through which certain suppliers could elect to receive advance payment from a designated finance company on invoices due to them by Gateway. Any difference between the original amount due to the supplier for the goods and/or services received and the amount ultimately required to be repaid by Gateway to the finance company, including fees and interest, is recorded as interest expense (or income, if applicable) for the period. Included in accounts payable is approximately \$44 million and \$30 million that was advanced to suppliers and outstanding to the finance company as of December 31, 2006 and 2005, respectively. On January 7, 2007 this program was discontinued.

(n) Deferred Stock-Based Compensation:

Gateway issued 5.3 million shares of restricted stock valued at approximately \$27 million to certain executives in connection with its acquisition of eMachines. This amount was recorded as deferred stock-based compensation and is being amortized to compensation expense in accordance with the vesting schedule. Approximately 2.1 million and 2.5 million shares vested on January 1, 2006 and 2005, respectively. During the second quarter of 2005, vesting on approximately 0.4 million shares was accelerated for a departing executive, resulting in an additional compensation charge of \$1.3 million. The remaining 0.3 million shares vested on January 1, 2007. Deferred stock based compensation was \$2.7 million as of December 31, 2006.

(o) Revenue Recognition:

Gateway recognizes revenue on PCs, servers and Non-PC products when persuasive evidence of an arrangement exists, delivery has occurred, the sales price is fixed and determinable, and collectibility is reasonably assured. Revenue from training services are recognized as the services are provided. Revenue from Internet access, web portals, and security services provided by third parties is recognized as the services are

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GATEWAY, INC.

NOTES TO CONSOLIDATED FINANCIAL STATEMENTS—(Continued)

provided based on subscriber counts reported to us by the service providers. If the actual subscriber counts or the economics associated with these subscriber counts prove to be more or less than originally reported by the service providers, Gateway may be required to adjust revenue. In the fourth quarter of 2002, America Online, Inc. ("AOL") unilaterally recomputed payments it had made in 2001 and the first half of 2002 and withheld the claimed overpayments from amounts currently owed to Gateway. Gateway disputed AOL's retroactive adjustment and reached a settlement in November 2004 for \$2.5 million related to the contested period and an additional \$1.6 million for subsequent periods through 2004. This was recognized as revenue in 2004. Revenue from the sale of other services rendered by third parties, such as installation services, is generally recognized when such services are performed.

Gateway records reductions in revenue in the current period for estimated future product returns and estimated rebate redemption rates related to current period sales. Management analyzes historical returns, current trends, changes in customer demand and acceptance of our products when evaluating the adequacy of the sales returns allowances in any accounting period. Management also analyzes historical rebate redemption rates, current trends and the interrelationship of these rates with the current rebate dollar amounts in evaluating rebate allowances. If actual returns exceed estimated returns or if actual rebate redemptions exceed estimates, we would be required to record additional reductions to revenue which would affect earnings in the period the adjustments are made. Gateway also records reductions to revenue for estimated commitments related to other customer and sales incentive programs. This includes, among other things, trade-ins and referral credits. Future market conditions and product transitions may require us to increase customer incentive programs that could result in incremental reductions of revenue at the time such programs are offered, which would affect earnings in the period the adjustments are made. Gateway recorded the following amounts against revenue for rebates for 2006, 2005, and 2004 of \$16 million, \$69 million, and \$105 million, respectively. Gateway recorded the following amounts against revenue for returns for 2006, 2005, and 2004 of \$188 million, \$186 million, and \$226 million, respectively.

Gateway offers its customers an option to purchase extended warranties. Revenue related to sales of extended warranties sold on behalf of third-parties is recognized at the time of sale, net of amounts due to the third-party. Revenue from sales of extended warranties where Gateway is the legal obligor is deferred and recognized on a straight-line basis over the warranty service period. Gateway expects that deferred revenue, and the revenue stream associated with it, will continue to decline in future quarters. A schedule of additions to extended warranty deferred revenue which is included in other liabilities and other long-term liabilities and recognition of extended warranty revenue for the periods presented is as follows (in thousands):

	<u>2006</u>	<u>2005</u>
Extended warranty deferred revenue, beginning of the period	\$ 87,806	\$ 178,381
Additions to extended warranty deferred revenue	10,885	23,193
Extended warranty revenue recognized	<u>(58,652)</u>	<u>(113,768)</u>
Extended warranty deferred revenue, end of the period	<u>\$ 40,039</u>	<u>\$ 87,806</u>

Gateway records revenue net of sales taxes or valued-added taxes levied by governmental authorities. Such taxes are considered current liabilities and included within accrued expenses until paid.

(p) **Market Development Funds:**

Gateway receives funding from various suppliers generically known as market development funds ("MDF") to encourage it to utilize certain components in the design or manufacture of its products, provide pass-through sales incentives to Gateway's customers, or reimburse Gateway for a portion of its qualifying advertising or sales

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GATEWAY, INC.

NOTES TO CONSOLIDATED FINANCIAL STATEMENTS—(Continued)

efforts. Typically the vendor allocates these funds to Gateway based on purchase volumes. Gateway considers these funds earned and recognizes these arrangements when substantially all of the vendors' requirements for funding have been satisfied and collection is assured. If the underlying vendor requirement specifies that Gateway incur or spend for qualifying advertising or sales efforts, these funds are offset against selling, general, and administrative expense, otherwise they are offset against cost of goods sold in the period earned.

(q) Shipping and Handling:

Shipping and handling costs are included in costs of sales for all periods presented. Shipping and handling costs charged to customers is recorded as revenue in the period the related product sales revenue is recognized.

(r) Advertising Costs:

Advertising costs, net of market development funds reimbursement, are charged to expense as incurred and are included within selling, general and administrative expenses. Net advertising expenses were approximately \$41 million, \$57 million, and \$79 million for 2006, 2005, and 2004, respectively.

(s) Income Taxes:

The provision or benefit for income taxes is computed using the liability method, under which deferred tax assets and liabilities are recognized for the expected future tax consequences of temporary differences between the financial reporting and tax bases of assets and liabilities. Deferred tax assets are reduced by a valuation allowance when it is more likely than not that some portion or all of the deferred tax assets will not be realized. Other current liabilities include tax liabilities related to current or future federal, state or foreign tax audits. See Note 6.

(t) Net Income (Loss) Per Share:

Basic income (loss) per common share is computed using net income (loss) attributable to common stockholders and the weighted average number of common shares outstanding during the period. Diluted income (loss) per common share (if applicable) is computed using net income (loss) attributable to common stockholders, as adjusted, and the combination of the weighted average number of common shares outstanding and all potentially dilutive common shares outstanding during the period unless the inclusion of such shares is anti-dilutive.

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GATEWAY, INC.

NOTES TO CONSOLIDATED FINANCIAL STATEMENTS—(Continued)

The following table sets forth the computation of basic and diluted income (loss) per share for 2006, 2005, and 2004 (in thousands, except per share amounts):

	2006	2005	2004
Basic net income (loss) per share calculation:			
Net income (loss) attributable to common stockholders—basic	\$ 9,643	\$ 6,161	\$(475,476)
Weighted average shares outstanding—basic	<u>373,001</u>	<u>371,661</u>	<u>363,708</u>
Basic net income (loss) per share	<u>\$ 0.03</u>	<u>\$ 0.02</u>	<u>\$ (1.31)</u>
Diluted net income (loss) per share calculation:			
Net income (loss) attributable to common stockholders—basic	\$ 9,643	\$ 6,161	\$(475,476)
Preferred stock dividends and accretion	—	—	7,991
Gain on redemption of preferred stock	—	—	(100,133)
Net income (loss) attributable to common stockholders—diluted	<u>\$ 9,643</u>	<u>\$ 6,161</u>	<u>\$(567,618)</u>
Weighted average shares outstanding—basic	<u>373,001</u>	<u>371,661</u>	<u>363,708</u>
Series A preferred stock	—	—	21,631
Series C preferred stock	—	—	5,776
Stock options	<u>1,022</u>	<u>506</u>	<u>—</u>
Weighted average shares outstanding—diluted	<u>374,023</u>	<u>372,167</u>	<u>391,115</u>
Diluted net income (loss) per share	<u>\$ 0.03</u>	<u>\$ 0.02</u>	<u>\$ (1.45)</u>

The 2004 gain on redemption of the Series A and C preferred stock is included in net income attributable to common shareholders in accordance with EITF Topic D-42 but excluded from the calculation of diluted earnings per share under the “if-converted” method of SFAS 128, “Earnings Per Share”. Diluted shares for 2004 excludes 3,145 weighted average incremental shares related to employee and director stock options despite their exercise prices being below the average market price of Gateway common stock as their effect on loss per share is anti-dilutive. Diluted shares also excludes 34,762 shares related to the senior convertible notes in 2006, 2005 and 2004, as their effect is anti-dilutive. Gateway has also excluded from diluted loss per share 26,942 shares, 51,509 shares, and 52,112 shares for 2006, 2005, and 2004, respectively, related to employee and director stock options and non-employee warrants which have exercise prices greater than the average market price of the common shares for those periods.

(u) Stock-based Compensation:

Gateway’s Compensation Committee of the Board of Directors approved the accelerated vesting on October 4, 2005 of all unvested options held by then employees, directors and officers which had exercise prices greater than \$2.84 per share. Because these options had exercise prices significantly in excess of Gateway’s stock price of \$2.84 on the date of approval, Gateway believed that these options did not provide sufficient incentive to the employees when compared with the potential future compensation expense that would have been attributable to these options. The acceleration resulted in the recognition of an additional \$54 million pro-forma pre-tax stock based compensation in 2005. In accordance with current accounting guidance, this acceleration eliminated the compensation expense Gateway would otherwise recognize in its statement of operations with respect to these options with the implementation of SFAS 123-R in 2006.

On October 4, 2005, 2.0 million shares of restricted stock were granted to employees. These shares vest in four equal annual installments. A deferred compensation liability of \$5.6 million was recorded in the fourth quarter of 2005 balance sheet in association with this restricted stock grant.

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GATEWAY, INC.

NOTES TO CONSOLIDATED FINANCIAL STATEMENTS—(Continued)

On March 3, 2006, an executive received a grant of 93,023 shares of restricted stock which vests in 1 year. On September 18, 2006, an executive received a grant of 79,275 shares of restricted stock which vests in 3 equal installments. A deferred compensation liability of \$0.4 million was recorded in the 2006 balance sheet in association with these restricted stock grants.

Prior to the adoption of SFAS 123-R in 2006, Gateway measured compensation expense for its employee and non-employee director stock-based compensation using the intrinsic value method. Compensation charges related to other non-employee stock-based compensation are measured using fair value methods. The fair value of options was estimated on the date of grant using the Black-Scholes option pricing model with the following assumptions for the periods indicated:

	For the Year Ended December 31,		
	2006	2005	2004
Dividend yield			
Risk-free interest rate	5%	4%	4%
Expected volatility	56%	67%	80%
Expected option term (after vesting)	3.5 years	3.5 years	3.5 years

Had compensation expense for employee and director stock options been determined based on the fair value of the options on the date of the grant based on the assumptions outlined in Note 8 and applying graded vesting, net income (loss) and net income (loss) per share for 2005 and 2004 would have resulted in the following pro forma amounts (in thousands, except per share amounts):

	2005	2004
Net income (loss) attributable to common stockholders—as reported	\$ 6,161	\$(475,476)
Add: compensation expense included in net income, net of related tax effects	13,438	13,617
Deduct: Total stock-based employee compensation expense determined under fair value based method for all awards, net of related tax effects	(74,278)	(46,937)
Net income (loss) attributable to common stockholders—pro forma	<u>\$(54,679)</u>	<u>\$(508,796)</u>
Basic net income (loss) per share—as reported	\$ 0.02	\$ (1.31)
Basic net income (loss) per share—pro forma	<u>\$ (0.15)</u>	<u>\$ (1.40)</u>
Diluted net income (loss) per share—as reported	\$ 0.02	\$ (1.45)
Diluted net income (loss) per share—pro forma	<u>\$ (0.15)</u>	<u>\$ (1.54)</u>

(v) Treasury Stock:

Gateway has acquired shares of its common stock which are held in treasury. This includes 2.7 million shares repurchased during the fourth quarter of 2004 in connection with the repurchase of the Series A and Series C preferred stock from America Online, Inc. In March 2004, Gateway issued 5.3 million shares of restricted stock to certain executives in connection with its acquisition of eMachines. In January 2005, approximately 2.5 million of these shares vested and Gateway issued 1.4 million shares of unrestricted stock (subject to certain limitations on disposition) and withheld the remaining 1.1 million shares to assist the executives in meeting certain tax liabilities associated with such vesting. During the second quarter of 2005, vesting on approximately 0.4 million restricted shares was accelerated for a departing executive. Approximately 0.2 million shares of these 0.4 million shares were withheld to assist the executive in meeting certain tax liabilities associated with vesting. During 2006, approximately 2.1 million of the originally issued shares of restricted stock vested and Gateway

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NOTES TO CONSOLIDATED FINANCIAL STATEMENTS—(Continued)

issued 1.1 million shares of unrestricted stock (subject to certain limitations on disposition) and withheld the remaining 1.0 million shares to assist the executives in meeting certain tax liabilities associated with such vesting. In June 2006, Gateway repurchased approximately 0.2 million shares of common stock in a private transaction from a Gateway executive at a price equal to the market price as of the date of purchase. In October 2006, Gateway withheld approximately 0.1 million shares on the vesting of employee restricted stock. All shares withheld to cover tax liabilities are valued at their fair market value on the vesting date and are included in treasury stock. Treasury stock is accounted for under the cost method and is available for issuance. Gateway acquired treasury stock for the above noted purchases and withholdings in the amount of \$7.5 million and \$3.2 million in 2005 and 2006, respectively.

(w) Foreign Currency:

Gateway considers the U.S. dollar to be its functional currency for certain of its international operations and the local currency for all others. For subsidiaries where the local currency is the functional currency, the assets and liabilities are translated into U.S. dollars at exchange rates in effect at the balance sheet date. Income and expense items are translated at the average exchange rates prevailing during the period. Gains and losses from translation are included in accumulated other comprehensive income. Gains and losses resulting from remeasuring monetary asset and liability accounts that are denominated in currencies other than a subsidiary's functional currency are included in other income, net and are not significant.

(x) Derivatives and Hedging:

All derivative transactions are accounted for under SFAS No. 133, *Accounting for Derivative Instruments and Hedging Activities*, which requires that the Company recognize all derivatives (including derivatives embedded in other contracts) as either assets or liabilities on the balance sheet and measure those instruments at fair value. The Company's derivative financial instruments consist of forward currency contracts. These contracts are recognized on the balance sheet at their fair value, which is the estimated amount at which they could be settled based on market rates. Unless special hedge accounting is applied, under SFAS No. 133, the gains and losses do not qualify for hedge accounting. As such, all gains and losses on these contracts are reported in earnings as Other income, net. As of December 31, 2006, the Company had several of these contracts all scheduled to mature before March 31, 2007.

(y) Segment Data:

Gateway reports segment data based on the internal reporting that is used by senior management for making operating decisions and assessing performance. Gateway's operating segments are Retail (including International), Professional, and Direct. The International segment currently meets the aggregation criteria of Statement of Financial Accounting Standards No. 131, "Disclosures about Segments of an Enterprise and Related Information" and is included in the Retail segment for external reporting purposes. See Note 11.

(z) New Accounting Pronouncements:

In September 2006, the SEC issued SAB No. 108, "Considering the Effects of Prior Year Misstatements when Quantifying Misstatements in Current Year Financial Statements" ("SAB 108"). SAB 108 provides guidance on the consideration of the effects of prior year misstatements in quantifying current year misstatements for the purpose of a materiality assessment. SAB 108 establishes an approach that requires quantification of financial statement errors based on the effects of each of the company's balance sheet and statement of operations and the related financial statement disclosures. Early application of the guidance in SAB 108 is encouraged in any report for an interim period of the first fiscal year ending after November 15, 2006, and was adopted by Gateway in the fourth quarter of fiscal 2006. The adoption of SAB 108 did not have a material impact on Gateway's consolidated results of operations, financial position or cash flows.

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In September 2006, the FASB issued SFAS No. 157, "Fair Value Measurements" ("SFAS 157"). SFAS 157 provides guidance for using fair value to measure assets and liabilities. It also responds to investors' requests for expanded information about the extent to which companies measure assets and liabilities at fair value, the information used to measure fair value, and the effect of fair value measurements on earnings. SFAS 157 applies whenever other standards require (or permit) assets or liabilities to be measured at fair value, and does not expand the use of fair value in any new circumstances. SFAS 157 is effective for financial statements issued for fiscal years beginning after November 15, 2007 and is required to be adopted by Gateway in the first quarter of fiscal 2009. Management does not believe the adoption of SFAS 157 will have a material impact on Gateway's consolidated results of operations, financial position or cash flows.

In July 2006, the FASB issued FASB Interpretation No. 48, "Accounting for Uncertainty in Income Taxes, an interpretation of FASB Statement No. 109" ("FIN 48"). FIN 48 clarifies the accounting for uncertainty in income taxes by prescribing the recognition threshold a tax position is required to meet before being recognized in the financial statements. It also provides guidance on derecognition, classification, interest and penalties, accounting in interim periods, disclosure, and transition. FIN 48 is effective for fiscal years beginning after December 15, 2006 and is required to be adopted by Gateway in the first quarter of fiscal 2007. The cumulative effects, if any, of applying FIN 48 will generally be recorded as an adjustment to retained earnings as of the beginning of the period of adoption. Gateway is currently evaluating the effect that the adoption of FIN 48 will have on its consolidated results of operations and financial condition and is not yet in a position to finalize its determination of such effects.

In February 2006, the FASB issued SFAS No. 155, "Accounting for Certain Hybrid Financial Instruments—an amendment of FASB SFAS Nos. 133 and 140". This Statement amends FASB SFAS No. 133, "Accounting for Derivative Instruments and Hedging Activities", and No. 140, "Accounting for Transfers and Servicing of Financial Assets and Extinguishment of Liabilities". SFAS 155 resolves issues addressed in Statement 133 Implementation Issue No. D1, Application of Statement 133 to Beneficial Interests in Securitized Financial Assets. SFAS 155 is effective for all financial instruments acquired or issued after the beginning of an entity's first fiscal year that begins after September 15, 2006. Management does not believe the adoption of SFAS 155 will have a material impact on Gateway's consolidated results of operations, financial position or cash flows.

In September 2006, the FASB issued SFAS No. 158, "Employers' Accounting for Defined Benefit Pension and Other Postretirement Plans—An Amendment of FASB No. 87, 88, 106 and 132(R)" ("SFAS 158"). SFAS 158 requires that the funded status of defined benefit postretirement plans be recognized on the company's balance sheet, and changes in the funded status be reflected in comprehensive income, effective fiscal years ending after December 15, 2006. SFAS also requires companies to measure the funded status of the plan as of the date of its fiscal year-end, effective for fiscal years ending after December 15, 2008. Since Gateway does not currently have a defined benefit postretirement plan, the adoption of SFAS 158 did not have a material impact on Gateway's consolidated results of operations, financial position or cash flows.

2. Selected Balance Sheet Information (in thousands except where otherwise noted):

Gateway purchases selected components from suppliers and, where possible, in lieu of a consignment arrangement, resells the components to original design manufacturers to incorporate into products being manufactured for Gateway. The receivable for the sale of the components is recorded as "Receivables from suppliers", thus, such arrangements have the effect of increasing other current assets and decreasing inventory. The increase in "Receivables from suppliers" is attributable to Gateway using "buy-sell" arrangements with three additional original design manufacturers. Gateway has now moved all their original design manufacturers to this model.

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GATEWAY, INC.

NOTES TO CONSOLIDATED FINANCIAL STATEMENTS—(Continued)

The \$28 million increase in property plant, and equipment, net is due to \$52 million of additions in construction in progress (primarily major software projects placed in service in early 2007), and \$8 million of other equipment additions offset by \$19 million of depreciation expense, \$178 million of disposals of fully depreciated assets, and \$13 million of disposals related to the Kansas City facility closure (carrying value of \$25 million net of accumulated depreciation of \$12 million).

The \$27 million decrease in prepaid expenses consists of decreased prepaid royalties (\$15 million), decreased prepaid warranty expense (\$6 million), and other prepaid expenses (\$6 million).

The \$27 million increase in other assets consists of increased vendor rebate receivables (\$11 million), increased forward currency contracts (\$20 million), partially offset by a decrease in other current assets (\$4 million).

	2006	2005
Receivables from suppliers	\$ 247,207	\$ 213,901
Other current assets:		
Prepaid expenses	40,299	67,162
Assets held for sale	14,774	9,162
Other	160,509	133,527
	<u>\$ 215,582</u>	<u>\$ 209,851</u>
Property, plant and equipment, net:		
Land	\$ 1,904	\$ 1,904
Leasehold improvements	5,819	6,344
Buildings	26,746	40,149
Construction in progress	61,834	23,103
Internal-use software	205,848	248,325
Office and production equipment	32,290	152,350
Furniture and fixtures	7,090	12,047
Vehicles	45	313
	<u>341,576</u>	<u>484,535</u>
Less: Accumulated depreciation and amortization	<u>(230,645)</u>	<u>(401,379)</u>
Property, plant and equipment, net	<u>\$ 110,931</u>	<u>\$ 83,156</u>
Accumulated other comprehensive loss:		
Foreign currency translation	\$ (921)	\$ (1,025)
Unrealized loss on available-for-sale securities, net of taxes	(299)	(1,745)
	<u>\$ (1,220)</u>	<u>\$ (2,770)</u>

3. Financing Arrangements:

On October 30, 2004, Gateway entered into a credit agreement with a major financial institution to provide for a revolving credit facility of up to \$200 million. Borrowings under this agreement bear interest, at Gateway's election, based on LIBOR or the prime rate and are secured by substantially all of Gateway's accounts receivable, inventory and certain deposit accounts into which accounts receivable payments are initially deposited. In addition to usual and customary covenants for an arrangement of its type, the credit agreement includes certain financial covenants. Gateway renegotiated the credit agreement as of December 26, 2006 to

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replace the financial covenant that Gateway maintain a certified cash balance of \$150 million with covenants that Gateway maintain a liquidity position of \$100 million and negative cash flow not to exceed \$40 million and \$57 million for the fourth quarter of 2006 and the first quarter of 2007, respectively, and \$60 million for each quarter thereafter, with cumulative negative cash flow not to exceed \$120 million. Further, once Gateway has achieved 3 consecutive quarters of positive excess cash flow, the amended credit agreement requires that Gateway maintain positive cash flow in each quarter thereafter. The agreement expires on October 31, 2010, at which time all amounts then outstanding will be due and payable. During the second quarter of 2005, Gateway restructured approximately \$51 million of its letters of credit, guarantees, and controlled accounts which had previously been secured by restricted cash on deposit with financial institutions to letters of credit and guarantees secured by a \$47 million utilization of the letter of credit line under this revolving credit facility. As of December 31, 2006 and December 31, 2005, Gateway had \$0 and \$50 million, respectively in borrowings outstanding under this agreement. The interest rate as of December 31, 2006 was 7.25%. This interest rate adjusts with changes in the prime rate. We also utilized the credit agreement to support \$36 million of stand-by letters of credit and had borrowing availability of \$35 million.

In December 2004, Gateway completed the sale of \$300 million of senior convertible notes through a private placement to institutional investors, including \$150 million of 1.50% senior convertible notes due December 31, 2009 and \$150 million of 2.00% senior convertible notes due December 31, 2011. The notes are direct, unsecured and unsubordinated obligations of Gateway and rank equal in priority to Gateway's existing and future unsecured indebtedness and senior in right of payment to any future subordinated indebtedness. Each \$1,000 note is initially convertible into 115.8749 shares of Gateway common stock based on an initial conversion price of \$8.63, or approximately 34.8 million shares in aggregate, at anytime prior to the close of business on the business day immediately prior to scheduled maturity. Gateway may settle a conversion election in cash, common shares or a combination of both. Note holders who elect to convert upon the occurrence of any transaction or event in connection with which 90% or more of Gateway's common stock is exchanged for, converted into, acquired for or constitutes solely the right to receive, consideration which is not at least 90% common stock that is listed on a United States national securities exchange or approved for trading on the NASDAQ National Market may be entitled to receive additional shares of Gateway common stock based on established formulas. Gateway may not redeem the notes prior to maturity but note holders may require Gateway to repurchase all or a portion of the notes at 100% of principal plus accrued and unpaid interest upon occurrence of certain defined designated events. Interest is payable semi-annually each June 30 and December 31.

Gateway recorded interest expense of \$5.7 million, \$6.1 million, and \$0.8 million for 2006, 2005, and 2004, respectively.

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4. Marketable Securities and Long-Term Investments:

As of December 31, 2006 and 2005, the carrying value of Gateway's marketable securities and long-term investments is as follows (in thousands):

2006					
Cost	Gross Unrealized Gains	Gross Unrealized Losses— Less Than 1 Year	Gross Unrealized Losses— More than 1 Year	Other than Temporary Charges	Carrying Value
State and municipal securities	\$ —	\$ —	\$ —	\$ —	\$ —
Mortgage-backed securities	—	—	—	—	—
U.S. Government and agencies	31,775	(27)	(188)	(81)	31,479
Corporate debt securities	39,210	12	(35)	53	39,179
Total marketable securities	<u>\$70,985</u>	<u>\$ 12</u>	<u>\$ (62)</u>	<u>\$ (28)</u>	<u>\$70,658</u>
Long-term investments, at cost	<u>\$ 3,159</u>	<u>\$ —</u>	<u>\$ —</u>	<u>\$ —</u>	<u>\$ 3,159</u>

2005					
Cost	Gross Unrealized Gains	Gross Unrealized Losses— Less Than 1 Year	Gross Unrealized Losses— More than 1 Year	Other than Temporary Charges	Carrying Value
State and municipal securities	\$ 10,950	\$ —	\$ —	\$ —	\$ 10,950
Mortgage-backed securities	29,071	1	(330)	(220)	28,492
U.S. Government and agencies	74,306	1	(833)	(91)	73,344
Corporate debt securities	52,787	6	(513)	(1,851)	50,414
Total marketable securities	<u>\$167,114</u>	<u>\$ 8</u>	<u>\$ (1,676)</u>	<u>\$ (2,162)</u>	<u>\$163,200</u>
Long-term investments, at cost	<u>\$ 3,159</u>	<u>\$ —</u>	<u>\$ —</u>	<u>\$ —</u>	<u>\$ 3,159</u>

Unrealized losses in mortgage-backed, U.S. government and agency and corporate debt securities are largely due to recent interest rate increases. Management continues to monitor its marketable security portfolio but does not believe the unrealized losses as of December 31, 2006 and 2005 are other-than-temporary. As a result, no other-than-temporary impairment charges were recorded in 2006 or 2005. The following table summarizes debt maturities, excluding mortgage-backed securities which are not due on a single maturity date, at December 31, 2006 (in thousands):

	Amortized Cost	Carrying Value
Less than one year	\$ 20,034	\$20,315
Due in 2-3 years	32,596	32,214
Due in 4-5 years	13,375	13,271
Due after 5 years	4,980	4,858
	<u>\$ 70,985</u>	<u>\$70,658</u>

Gateway held no auction rate securities at December 31, 2006. At December 31, 2005, Gateway held approximately \$16 million in auction rate securities.

Table of Contents**GATEWAY, INC.****NOTES TO CONSOLIDATED FINANCIAL STATEMENTS—(Continued)****5. Commitments, Contingencies and Concentrations:****Commitments**

Gateway leases certain operating facilities and equipment under non-cancelable operating leases expiring at various dates through 2012. Rent expense excluding closed facilities under restructuring plans was approximately \$3 million, \$3 million, and \$11 million for 2006, 2005, and 2004, respectively. Gateway also subleases certain closed facilities.

Gateway has entered into licensing and royalty agreements that allow it to use certain hardware and software intellectual properties in its products. Total royalty expense in many cases is based on the number of units sold and actual amounts to be paid will be greater than the minimum amount stated in the table below.

Future minimum lease expense and sublease income under terms of non-cancelable operating lease and sublease agreements, including lease and sublease amounts associated with closed facilities which are included in restructuring liabilities, and minimum royalty expense under royalty agreements as of December 31, 2006 are as follows (in thousands):

<u>Years Ending December 31:</u>	<u>Lease Obligations</u>	<u>Sublease Income</u>	<u>Net Leases</u>	<u>Royalty Agreements</u>
2007	\$ 22,848	\$15,189	\$ 7,659	\$ 7,850
2008	21,236	13,446	7,790	7,152
2009	18,443	13,588	4,855	7,152
2010	16,578	14,021	2,557	7,152
2011	13,308	14,126	(818)	5,032
Thereafter	5,177	12,316	(7,139)	5,767
Total	<u>\$ 97,590</u>	<u>\$82,686</u>	<u>\$ 14,904</u>	<u>\$ 40,105</u>

Certain of Gateway's operating lease commitments have been accrued for in connection with its restructuring actions. See Note 13 for further information.

Contingencies

Gateway had stand-by letters of credit and guarantees outstanding at December 31, 2006 and 2005, amounting to \$36 million and \$47 million, respectively. Beginning in the second quarter of 2005, these letters of credit and guarantees are primarily issued through Gateway's revolving credit facility.

Gateway is a party to various lawsuits, claims, including assertions of patent infringements, investigations and administrative proceedings that arise in connection with its business, including those identified below. Gateway evaluates such matters on a case by case basis, and its policy is to vigorously contest any such claims it believes are without merit.

Litigation

Rattner v. Snyder, et al. is a derivative action filed on September 6, 2006, in California State Superior Court, County of Orange, against Gateway as a nominal defendant and against individual members of Gateway's board of directors. The suit alleges that Board members breached their fiduciary duties in connection with the Gateway's September 1, 2006 announcement that it had rejected an earlier offer by shareholder Lap Shun "John" Hui to acquire Gateway's retail operations for approximately \$450 million. The complaint seeks unspecified damages and declaratory relief. On November 13, 2006, Gateway filed a motion for an order compelling plaintiff

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NOTES TO CONSOLIDATED FINANCIAL STATEMENTS—(Continued)

to furnish a bond, pursuant to California Corp. Code § 800(c), and the court has yet to rule on Gateway's motion. The parties have stipulated that the director defendants need not appear in the matter or otherwise respond to the complaint until after a demand-futility motion to be filed by Gateway is resolved.

Lucent Technologies, Inc. v. Gateway, Inc. is a suit filed on June 6, 2002 in the United States District Court for the Eastern District of Virginia which was subsequently transferred to the United States District Court for the Southern District of California, asserting that Gateway infringes seven patents owned by Lucent Technologies, Inc. On or about February 26, 2003, Microsoft intervened in the action, seeking to challenge Lucent's allegations with respect to five of the seven patents. In addition, on April 8, 2003, Microsoft filed an action against Lucent in the United States District Court for the Southern District of California. The suit seeks declaratory judgment that Microsoft products do not infringe patents held by Lucent, including the five patents upon which Microsoft based its intervention in the action Lucent brought against Gateway. On February 20, 2003, Lucent also sued Dell Inc. in the United States District Court for the District of Delaware on six patents, all of which are included in Microsoft's declaratory judgment action, and several of which are asserted by Lucent against Gateway. The suit against Dell was subsequently transferred to the United States District Court for the Southern District of California, where all three actions have been consolidated for discovery purposes. Lucent subsequently filed amended complaints against Dell and Gateway, respectively, asserting the same patents against each company. Through its amendments, Lucent asserted one additional patent against Dell and four additional patents against Gateway. All of the patents added through amendment are at issue in the Microsoft declaratory judgment action. The Court began conducting a Markman hearing on the asserted patents in August 2003 and conducted over 30 days of hearings before concluding the Markman hearing in September 2005. In September 2005, the Court also granted a summary judgment of invalidity with respect to one of the Lucent patents asserted against Gateway. Discovery is complete. The three actions have been consolidated into five separate trials, in which a different group of patents will be tried to each jury. The first of those trials involved Microsoft only, and was related to audio patents not asserted against Gateway. On February 22, 2007, a jury returned a verdict of approximately \$1.5 billion against Microsoft. Microsoft is expected to appeal. The first trial that involves Gateway is scheduled to begin on March 19, 2007, with three additional trials expected to occur in 2007 and possibly 2008.

Dvorchak v. eMachines, Inc., et al. is a shareholder class action against eMachines, Inc. and others filed in November 2001, in California State Superior Court, County of Orange, relating to a 2001 transaction in which eMachines, which was then a public company, was taken private. The action originally sought to enjoin eMachines' merger with Empire Acquisition Corp. (the "Merger") to effectuate taking eMachines private. The court denied the requested injunction on December 27, 2001, allowing the consummation of the Merger. After the Merger, plaintiffs filed amended complaints seeking unspecified monetary damages and/or rescission relating to the negotiations for and terms of the Merger through allegations of breaches of fiduciary duties by eMachines, its board members prior to the Merger, and certain of its officers. The court granted class certification on August 25, 2003. Dispositive motions filed by the defendants were heard and denied by the Court in August 2004 and August 2005. No trial date has been set, but the trial is currently anticipated to occur sometime in 2007.

In accordance with SFAS No. 5, "Accounting for Contingencies," Gateway reserves for a legal liability when it is both probable that a liability has been incurred and the amount of the loss can be reasonably estimated. At least quarterly, Gateway reviews and adjusts these reserves to reflect the impacts of negotiations, settlements, rulings, advice of legal counsel and other information and events pertaining to a particular case. The ultimate outcome of such matters cannot presently be determined or estimated. Gateway's management believes that Gateway has sufficiently reserved for legal matters and that the ultimate resolution of pending matters will not have a material adverse impact on Gateway's consolidated financial position, operating results or cash flows. However, the results of legal proceedings cannot be predicted with certainty. Should Gateway fail to prevail in current legal matters or should one or more of these legal matters be resolved against Gateway, Gateway could be

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NOTES TO CONSOLIDATED FINANCIAL STATEMENTS—(Continued)

required to pay substantial monetary damages or, if injunctive relief is granted, may be prohibited from selling one or more of its products and, in either case, its operating results and cash flows could be materially adversely affected.

Concentrations

Gateway depends on many third-party suppliers, service providers and manufacturers for key products and components contained in its products and service solutions offerings. For some of these products and components, Gateway may only use a single source supplier, in part due to the lack of alternative sources of supply or to obtain favorable pricing. If the supply of a key product or component were to be delayed or curtailed, Gateway's ability to ship the related product or solution in desired quantities and in a timely manner could be adversely affected which, in turn would adversely affect Gateway's results of operations. In cases where alternative sources of supply are available, qualification of the sources and establishment of reliable alternate suppliers could result in delays and possibly adversely affect results of operations.

Gateway's retail segment sells its products to a limited number of third-party retailers. One retailer, Best Buy, accounted for 36%, 37% and 30% of accounts receivable, net as of December 31, 2006, 2005 and 2004, respectively, and 39%, 34% and 23% of consolidated net sales in 2006, 2005 and 2004, respectively.

Similarly, Gateway depends on third-party suppliers of its solutions offerings, including financing and Internet access. Should any of these sources discontinue the provision of services sold through Gateway or be less willing to offer their services to Gateway for any reason, then this would lead to a reduction in net sales if Gateway is unable to find alternative sources of these services.

Guarantees

During the normal course of business, Gateway makes certain indemnities, commitments and guarantees under which it may be required to make payments in relation to certain transactions. These include: (i) intellectual property indemnities to its customers and licensees in connection with the use, sales and/or license of its products, (ii) indemnities to vendors and service providers pertaining to claims based on the negligence or willful misconduct of Gateway and (iii) indemnities involving the accuracy of representations and warranties in certain contracts. The majority of these indemnities, commitments and guarantees do not provide for any limitation of the maximum potential for future payments Gateway could be obligated to make. In addition, Gateway has made contractual commitments to several employees providing for payments upon the occurrence of certain prescribed events. Gateway has not recorded any liability for these indemnities, commitments and other guarantees.

6. Income Taxes:

The components of the income tax benefit are as follows (in thousands):

	2006	2005	2004
Current			
United States	\$(24,856)	\$(10)	\$(14,113)
Foreign	456	—	—
Deferred			
Income tax benefit	<u>\$(24,400)</u>	<u>\$(10)</u>	<u>\$(14,113)</u>

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GATEWAY, INC.

NOTES TO CONSOLIDATED FINANCIAL STATEMENTS—(Continued)

A reconciliation of the income tax benefit and the amount computed by applying the federal statutory income tax rate to income (loss) before income taxes is as follows (in thousands):

	2006	2005	2004
Federal income tax at statutory rate	\$ (5,165)	\$ 2,153	\$(203,665)
Increase (decrease) in valuation allowance	3,108	(523)	215,514
State income tax, net of federal benefit	318	298	(11,638)
Change in tax accrual	(25,174)	(185)	(14,113)
Foreign provision with rate differential	1,596	—	—
Other, net	917	(1,753)	(211)
Income tax benefit	<u>\$(24,400)</u>	<u>\$ (10)</u>	<u>\$ (14,113)</u>

In 2006, Gateway recorded a tax benefit of \$24 million primarily representing a change in tax accrual of \$25 million, together with foreign tax refunds recognized of \$2.1 million, offset by foreign and state tax accruals from operations of \$2.8 million. The change in tax accrual consists primarily of the reversal of previously accrued tax liabilities resulting from various tax authority settlements of \$27 million and recognition of domestic tax refunds of \$6.0 million. The benefit was offset by \$6.2 million of interest accruals relating to previously accrued liabilities, and \$1.5 million of current year accruals established for anticipated tax liabilities. The domestic tax refunds and accrued tax liability reversals represent various settlements between Gateway and the Appeals Office of the Internal Revenue Service with respect to multiple domestic and international issues under audit. These agreements are still subject to review of the Joint Committee on Taxation. Gateway believes the review of the Joint Committee will not adversely impact the recognition of the benefit recorded for these agreements.

Deferred tax assets and deferred tax liabilities result from temporary differences in the following accounts (in thousands):

	2006	2005	2004
Deferred tax assets:			
Inventory	\$ 7,397	\$ 8,278	\$ 7,051
Accounts receivable	3,008	4,595	6,353
Accrued liabilities	74,557	74,085	56,155
Operating loss carryforwards	366,251	364,559	396,853
Property, plant and equipment	23,891	23,201	15,583
Intangible assets	9,154	—	—
Capital loss carryforwards	77,474	—	—
Investments	7,055	92,337	94,166
Other	13,617	13,617	13,617
Total deferred tax assets	582,404	580,672	589,778
Deferred tax liabilities:			
Intangible assets	—	(43,715)	(47,139)
Prepaid expenses	(3,939)	(3,939)	(12,419)
Other	(22,620)	(36,033)	(32,712)
Total deferred tax liabilities	(26,559)	(83,687)	(92,270)
Valuation allowance	(575,685)	(516,825)	(517,348)
Net deferred tax liabilities	<u>\$ (19,840)</u>	<u>\$ (19,840)</u>	<u>\$ (19,840)</u>

Gateway has federal and state net operating loss carryforwards of approximately \$816 million and \$1.8 billion, respectively. The federal net operating loss carryforwards begin to expire in 2023 and the state net operating loss carryforwards expire between 2007 and 2021, depending on each state's law.

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GATEWAY, INC.

NOTES TO CONSOLIDATED FINANCIAL STATEMENTS—(Continued)

Gateway has capital loss carryforwards in the amount of \$209 million. The capital loss carryforwards will begin to expire in 2007.

Gateway is subject to ongoing audits from various taxing authorities in the jurisdictions in which it does business and believes it has adequately provided for income tax issues not yet resolved. As of December 31, 2006, approximately \$90 million had been accrued to provide for such matters. Based on a consideration of all relevant facts and circumstances, the Company does not believe the ultimate resolution of tax issues for all open tax periods will have a materially adverse effect upon its future results of operations or financial condition.

Gateway has a valuation allowance of approximately \$576 million as of December 31, 2006 for net deferred tax assets because of the uncertainty regarding their realization. Gateway expects to maintain a full valuation allowance on future tax benefits until an appropriate level of profitability is sustained. Until an appropriate level of profitability is sustained, Gateway does not expect to recognize any significant tax benefits from future results of operations.

Gateway reviewed its deferred tax asset and liability balances in connection with the preparation of the 2006 consolidated financial statements and in preparation for the adoption of FIN 48. This review resulted in a change in estimates related to certain deferred tax assets and liabilities. Because the company has a valuation allowance, the change in estimate had no effect on the consolidated financial statements as of December 31, 2006.

Also included in Gateway's deferred tax asset and liability schedule above are excess tax deductions relating to stock options. When the benefit of the net operating losses containing these excess tax deductions are realized, the benefit will not affect the Statement of Operations, but rather additional paid in capital. For the year ended December 31, 2006 the excess tax deductions amount to \$5.3 million. These amounts have been excluded from the net operating loss carryforward. The cumulative amount of excess tax deductions presented in the net operating loss carryforward above from years 2001 through 2005 is \$8.2 million. To the extent that such excess tax deductions are realized in the future by virtue of reducing income taxes payable, the Company would expect to increase additional paid in capital by approximately \$4.7 million.

Undistributed earnings of the Company's foreign subsidiaries for which no U.S. federal or state liability has been recorded are considered to be indefinitely reinvested. Accordingly, no provision for U.S. federal and state income taxes or foreign withholding taxes has been provided on such undistributed earnings.

7. Preferred Stock and Preferred Share Purchase Rights Plan:

Gateway has 5,000,000 shares of preferred stock authorized for issuance in one or more series, at a par value of \$.01 per share. In conjunction with the distribution of Preferred Share Purchase Rights, Gateway's Board of Directors designated 1,000,000 shares of preferred stock as Series B Junior Participating Preferred Stock and reserved such shares for issuance upon exercise of the Preferred Share Purchase Rights. As of December 31, 2006, 2005 and 2004 no shares of Series B Junior Participating Preferred Stock were outstanding.

On January 19, 2000, the Board of Directors implemented a Preferred Share Purchase Rights Plan (Rights Plan) to protect stockholders' rights in the event of a proposed non-consensual takeover of Gateway believed not to be in the stockholders' best interests. Under the Rights Plan, Gateway declared a dividend of one preferred share purchase right (a Right) for each share of Gateway's common stock outstanding. Pursuant to the Rights Plan, each Right entitles the registered holder to purchase from Gateway one one-thousandth of a share of Series B Junior Participating Preferred Stock, \$.01 par value per share, at a purchase price of \$350. In general, with certain exceptions, the Rights are exercisable only if a person or group (an Acquiring Person) acquires beneficial ownership of 15% or more of Gateway's outstanding shares of common stock. Upon exercise, holders, other than

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NOTES TO CONSOLIDATED FINANCIAL STATEMENTS—(Continued)

the Acquiring Person, will have the right, subject to termination, to receive Gateway's common stock or other securities, cash or other assets having a market value, as defined, equal to twice such purchase price. The Rights, which expire on January 18, 2010, are redeemable in whole, but not in part, at Gateway's option for a price of \$0.001 per Right. Under an agreement with a stockholder group, the Board of Directors agreed to review the Rights Plan before the 2007 annual meeting of stockholders.

During 1999, Gateway entered into a strategic relationship with America Online, Inc. ("AOL") to leverage certain of the companies' sales and distribution channels and capabilities. Under this agreement, Gateway sold \$200 million of common stock to AOL, issued 50,000 shares of non-voting Series C Redeemable Convertible Preferred Stock ("Series C Preferred Stock") and issued 50,000 shares of non-voting Series A Convertible Preferred Stock ("Series A Preferred Stock") in exchange for \$600 million in cash and shares of AOL.

On December 22, 2004, Gateway repurchased from AOL all of the outstanding Series A and Series C Preferred Stock plus 2.7 million shares of common stock for \$316 million. Consideration included \$280 million in cash to AOL and the application of a \$36 million credit towards amounts due to Gateway from AOL. The Company recognized a \$100 million gain available for common shareholders on the repurchase of the preferred stock. This gain was included in net income attributable to common shareholders in accordance with EITF Topic D-42 but excluded from the calculation of diluted earnings per share under the "if-converted" method of SFAS 128, "Earnings Per Shares." As of December 31, 2004, the Series A and C preferred shares were cancelled and the 2.7 million shares of common stock are held in treasury.

8. Stock Option Plans, Employee Stock Purchase Plan, Restricted Stock and Warrants:

Gateway maintains various stock option plans for its employees. Employee options are granted at the fair market value of the common stock at the date of grant. These options generally vest over a four-year period from the date of grant. In addition, these options generally expire, if not exercised, ten years from the date of grant. Gateway also maintains option plans for non-employee directors. Option grants to non-employee directors generally have an exercise price equal to the fair market value of the common stock on the date of grant. These options generally vest over one to three-year periods and generally expire, if not exercised, ten years from the date of grant.

Gateway's Compensation Committee of the Board of Directors approved the accelerated vesting on October 4, 2006 of all unvested options held by then employees, directors and officers which had exercise prices greater than \$2.84 per share. Because these options had exercise prices significantly in excess of Gateway's stock price of \$2.84 on the date of approval, Gateway believed that these options did not provide sufficient incentive to the employees when compared with the potential future compensation expense that would have been attributable to these options. The acceleration resulted in the recognition of an additional \$54 million pro-forma pre-tax stock based compensation in 2005.

For all of Gateway's stock option plans, options for 24,441,000 shares, 51,226,000 shares, and 21,933,000 shares of common stock were exercisable as of December 31, 2006, 2005 and 2004, respectively, with a weighted-average exercise price of \$11.57, \$9.76, and \$20.53, respectively. There were 40,468,000 shares, 24,489,000 shares, and 21,113,000 shares of common stock reserved and available for future grant under Gateway's stock option plans as of those dates, respectively.

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NOTES TO CONSOLIDATED FINANCIAL STATEMENTS—(Continued)

The following table summarizes activity under the stock option plans for 2006, 2005 and 2004 (in thousands, except per share amounts):

	Shares (in thousands)	Weighted- average exercise price	Weighted- Average remaining contractual term (in years)	Aggregate intrinsic value (in thousands)
Outstanding, January 1, 2004	52,730	\$ 15.29		
Granted	35,092	5.07		
Exercised	(2,959)	3.94		
Forfeited	(21,258)	14.18		
Outstanding, December 31, 2004	63,605	10.50	4.33	\$ —
Granted	9,172	4.24		
Exercised	(380)	2.88		
Forfeited	(16,518)	11.60		
Outstanding, December 31, 2005	55,879	9.20	3.16	\$ —
Granted	12,276	1.91		
Exercised	(38)	2.46		
Forfeited	(30,800)	7.41		
Outstanding, December 31, 2006	37,317	\$ 8.28	6.26	\$ —
Vested or expected to vest, December 31, 2006	34,599	\$ 8.77	6.05	\$ —
Options exercisable, December 31, 2006	24,441	\$ 11.57	4.89	\$ —

The weighted average fair value of options granted during 2006, 2005, and 2004 is \$0.87, \$2.15, and \$2.90 respectively. The aggregate intrinsic value of options outstanding at December 31, 2006 was calculated as the difference between the exercise price of the underlying options and the market price of our common stock for the 37.3 million shares that had exercise prices that were lower than the \$2.01 market price of our common stock at December 31, 2006. The total intrinsic value of options exercised during 2006, 2005, and 2004 was \$0, \$0.4 million, and \$4.4 million respectively, determined as of the date of exercise.

The following table summarizes information about Gateway's Common Stock options outstanding as of December 31, 2006 (in thousands, except per share amounts):

Range of Exercise Prices	Options Outstanding			Options Exercisable	
	Number Outstanding	Weighted-Average Remaining Contractual Life	Weighted-Average Exercise Price	Number Exercisable	Weighted-Average Exercise Price
\$ 0.00-\$ 8.25	31,306	7.00	\$ 3.69	18,430	\$ 4.85
\$ 8.25-\$16.50	670	0.64	14.67	670	14.67
\$16.50-\$24.75	2,217	2.78	20.02	2,217	20.02
\$24.75-\$33.00	1,534	2.06	31.17	1,534	31.17
\$33.00-\$41.25	10	2.28	35.81	10	35.81
\$41.25-\$49.50	297	2.87	44.63	297	44.63
\$49.50-\$57.75	699	2.72	55.02	699	55.02
\$57.75-\$66.00	9	3.18	63.95	9	63.95
\$66.00-\$74.25	575	3.31	67.38	575	67.38
Totals	37,317	6.26	8.28	24,441	11.57

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NOTES TO CONSOLIDATED FINANCIAL STATEMENTS—(Continued)

The fair value of these options was estimated on the date of grant, with the following assumptions used under the Black-Scholes option pricing model:

	For the Year Ended December 31,		
	2006	2005	2004
Dividend yield	—	—	—
Risk-free interest rate	5%	4%	4%
Expected volatility	56%	67%	80%
Expected option term (after vesting)	3.5 years	3.5 years	3.5 years

Gateway offered eligible employees the opportunity to acquire shares under an employee stock purchase plan. Under the plan, shares of Gateway's common stock may be purchased at 100% of fair market value around the last business day of each month. Employees could purchase shares having a value up to 20% of their salary, subject to certain statutory limits. Total shares purchased for participating employees under the plan were 4,359 shares, 38,740 shares, and 65,894 shares for 2006, 2005, and 2004, respectively. Employee withholdings under the plan were terminated effective December 31, 2005 and the plan was terminated effective October 24, 2006.

On October 4, 2005, 2.0 million shares of restricted stock were granted to employees. These shares vest in four equal annual installments.

On March 3, 2006, an executive received a grant of 93,023 shares of restricted stock which vests in 1 year. On September 18, 2006, an executive received a grant of 79,275 shares of restricted stock which vests in 3 equal installments. A deferred compensation liability of \$0.4 million was recorded in the 2006 balance sheet in association with these restricted stock grants.

The following table summarizes information about Gateway's restricted stock outstanding as of December 31, 2006 and 2005 (in thousands, except per share amounts):

	Number of shares (in thousands)	Price per share	Grant value	Weighted average remaining contractual term	Aggregate intrinsic value (in thousands)
Outstanding, January 1, 2004	—	\$ —	\$ —	—	\$ —
Granted	5,307	5.19	27,544		
Restriction Lapse	—	—	—		
Forfeited	—	—	—		
Outstanding, December 31, 2004	5,307	5.19	27,544	1.16	31,896
Granted	1,982	2.84	5,629		
Restriction Lapse	(2,904)	5.19	(15,069)		
Forfeited	(103)	2.84	(294)		
Outstanding, December 31, 2005	4,282	4.16	17,810	1.74	10,748
Granted	172	2.05	353		
Restriction Lapse	(2,499)	4.86	(12,143)		
Forfeited	(583)	2.84	(1,656)		
Outstanding, December 31, 2006	1,372	\$ 3.18	\$ 4,364	2.06	\$ 2,757
Vested or expected to vest, December 31, 2006	6,540	\$ 4.73	\$ 30,936	0.34	\$ 24,998

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Gateway issued warrants to purchase 850,191 shares of common stock at \$5.97 per share in exchange for certain consulting services during 2002. These warrants expired unexercised on April 5, 2006. Prior to 2002, Gateway had issued warrants to purchase 624,750 shares of common stock at \$8.92 per share. These warrants expired on September 4, 2005.

9. Retirement Savings Plan:

Gateway has a 401(k) defined contribution plan, which covers employees who have attained 18 years of age. Employees are eligible to participate on the first day of employment and may contribute up to 50% of their compensation to the plan in any plan year, subject to certain tax limitations. Participants receive a 50% matching employer contribution of up to 6% of their annual eligible compensation which vests over two years. Gateway made matching contributions of \$2.8 million, \$2.7 million, and \$3.6 million during 2006, 2005, and 2004, respectively.

10. Acquisition:

On March 11, 2004, Gateway completed its acquisition of eMachines, Inc., a privately-held PC company. The acquisition combined Gateway's Professional and Consumer (now called "Direct") businesses, scale and cash availability with eMachines' low cost structure, profitability, PC market strength, third-party retail network, and international presence. These factors contributed to a purchase price in excess of the fair value of eMachines' net tangible and intangible assets acquired and, as a result, Gateway recorded goodwill in connection with this transaction.

The total purchase price of \$262 million consisted of \$41 million of cash, approximately \$215 million in common stock and direct transaction costs of approximately \$6 million. The consideration included approximately 5.3 million shares of restricted common stock issued to certain members of eMachines' management and contingent upon continued employment of five of these executives through 2005 and two of these executives through 2006. The value of the common stock was determined based on the average market price of Gateway's common stock over the 2-day period prior to and 2-day period following January 30, 2004, the date the acquisition was announced. The value assigned to the restricted shares was approximately \$27 million and will continue to be amortized to operating expense through 2007. The unamortized balance as of December 31, 2006 associated with the restricted shares is shown in Deferred stock-based compensation in the accompanying consolidated balance sheet.

The purchase price was allocated to the identifiable assets acquired and liabilities assumed based on the fair value of eMachines' assets and liabilities as follows (in thousands):

Cash acquired	\$ 3,589
Tangible assets acquired	304,524
Amortizable intangible assets (customer relationships)	48,450
Indefinite-lived intangible assets (trademarks/trade names)	49,600
Goodwill	155,619
Liabilities assumed	(300,064)
Total consideration	<u>\$ 261,718</u>

The amortizable intangible assets consisting of customer-related intangible assets were assigned an estimated useful life of 10 years which will create approximately \$4.8 million in additional amortization expense annually through 2014. Goodwill represents the excess of the purchase price over the fair value of the net

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tangible and intangible assets acquired and is not tax deductible. Goodwill will not be amortized and will be tested for impairment at least annually or whenever events or circumstances indicate an event of impairment may exist.

Goodwill has been assigned to the Retail reporting segment which is consistent with the segment presentation of eMachines' activities.

The results of operations of eMachines have been included in Gateway's consolidated statements of operations since the completion of the acquisition on March 11, 2004. The following unaudited pro forma information presents a summary of the results of operations of Gateway assuming the acquisition of eMachines occurred on January 1, 2004 (in thousands, except per share amounts):

	2004
Net sales	\$3,984,264
Net loss attributable to common stockholders	\$ (463,139)
Basic loss per share	\$ (1.24)
Diluted loss per share	\$ (1.39)

11. Segment Data:

Gateway's segment sales and operations are delineated by operating segment as follows:

- **Retail**—includes sales through third-party retail channels of both eMachines and Gateway-branded products;
- **International**—includes international sales and is currently aggregated within the Retail segment for external reporting purposes as it meets the aggregation criteria of SFAS 131, Disclosures about Segments of an Enterprise and Related Information;
- **Professional**—includes sales to educational institutions (K-12 and higher education), government entities (federal, state and local), small-to-medium businesses, value-added resellers and certain other resellers; and
- **Direct**—includes consumer and small business sales generated via Gateway's web and phone centers as well as legacy revenue streams from Gateway's closed retail stores.

Revenues from these segments are derived from sales of PC and Non-PC products and services. Gateway evaluates the performance of its segments based on sales gross profit, and segment contribution, but does not allocate segment assets or other income and expense items for management reporting purposes. Segment contribution includes selling, general and administrative expenses and other overhead charges directly attributable to the segment and excludes certain expenses managed outside the reporting segment, including corporate selling, general and administrative expenses, the Microsoft benefit, depreciation and amortization, and the restructuring, transformation and integration charges discussed in Note 13.

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GATEWAY, INC.

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The following table presents revenue and operating income information by segment (in thousands):

	2006	2005	2004
Net sales:			
Retail (including International)	\$2,739,884	\$2,358,669	\$1,485,715
Professional	895,774	986,943	1,114,493
Direct	345,145	508,449	1,049,526
	<u>\$3,980,803</u>	<u>\$3,854,061</u>	<u>\$3,649,734</u>
Segment gross profit:			
Retail (including International)	\$ 118,050	\$ 137,076	\$ 57,712
Professional	62,189	91,399	141,300
Direct	75,122	93,962	194,049
	<u>\$ 255,361</u>	<u>\$ 322,437</u>	<u>\$ 393,062</u>
Segment contribution:			
Retail (including International)	\$ 96,350	\$ 120,536	\$ 43,161
Professional	(6,509)	16,937	58,356
Direct	35,379	41,601	25,070
	<u>\$ 125,220</u>	<u>\$ 179,074</u>	<u>\$ 126,587</u>
Non-segment expenses and other charges	(178,607)	(220,214)	(728,565)
Microsoft benefit	34,500	40,500	—
Consolidated operating loss	<u>\$ (18,887)</u>	<u>\$ (640)</u>	<u>\$ (601,978)</u>

The following table presents a reconciliation of segment operating income to consolidated income (loss) before income taxes (in thousands):

	2006	2005	2004
Segment operating income	\$ 125,220	\$ 179,074	\$ 126,587
Non-segment operating expenses:			
Restructuring and other charges:			
Cost of goods sold	—	86	(85,986)
Selling, general and administrative expenses	(479)	(13,144)	(391,704)
Other non segment operating expenses	(178,118)	(207,155)	(250,875)
Microsoft benefit	34,500	40,500	—
Other income, net	4,138	6,791	20,247
Minority interest	(18)	—	—
Consolidated income (loss) before income taxes	<u>\$ (14,757)</u>	<u>\$ 6,151</u>	<u>\$ (581,731)</u>

The following table presents net sales by major group of products and services (in thousands):

	2006	2005	2004
Desktops	\$1,868,312	\$1,894,172	\$1,982,141
Notebooks	1,437,016	1,191,898	790,159
Servers and other	32,129	57,392	54,474
Total personal computers (PC)	<u>3,337,457</u>	<u>3,143,462</u>	<u>2,826,774</u>
Non-PC	643,346	710,599	822,960
Consolidated net revenues	<u>\$3,980,803</u>	<u>\$3,854,061</u>	<u>\$3,649,734</u>

Table of Contents**GATEWAY, INC.****NOTES TO CONSOLIDATED FINANCIAL STATEMENTS—(Continued)**

Gateway had long-lived assets of \$111 million, \$83 million, and \$103 million as of December 31, 2006, 2005, and 2004, respectively.

Best Buy accounted for approximately 36%, 37% and 30% of accounts receivable, net, as of December 31, 2006, 2005 and 2004, respectively, and 39%, 34% and 23% of consolidated net sales for the year ended December 31, 2006, 2005 and 2004, respectively.

12. Selected Quarterly Financial Data (Unaudited):

The following tables contain selected unaudited consolidated quarterly financial data for Gateway for the periods indicated (in thousands, except per share data):

	<u>1st Quarter</u>	<u>2nd Quarter</u>	<u>3rd Quarter</u>	<u>4th Quarter</u>
Year Ended December 31, 2006:				
Net sales	\$1,077,822	\$ 919,312	\$ 963,162	\$1,020,506
Gross profit	78,728	50,576	73,370	52,687
Operating (loss) income	(15,743)	(6,948)	7,929	(4,114)
Net (loss) income	(12,335)	(7,680)	18,170	11,489
Basic net (loss) income per share	(0.03)	(0.02)	0.05	0.03
Diluted net (loss) income per share	(0.03)	(0.02)	0.05	0.03
Basic weighted average shares outstanding	372,982	372,089	371,846	371,690
Diluted weighted average shares outstanding	372,982	372,089	407,612	372,429

	<u>1st Quarter</u>	<u>2nd Quarter</u>	<u>3rd Quarter</u>	<u>4th Quarter</u>
Year Ended December 31, 2005:				
Net sales	\$ 837,781	\$ 873,112	\$1,018,973	\$1,124,194
Gross profit	80,365	87,414	84,693	69,966
Operating (loss) income	(7,761)	17,620	18,765	(29,263)
Net (loss) income	(5,186)	17,188	15,061	(20,902)
Basic net (loss) income per share	(0.01)	0.05	0.04	(0.06)
Diluted net (loss) income per share	(0.01)	0.05	0.04	(0.05)
Basic weighted average shares outstanding	371,152	371,198	371,166	373,115
Diluted weighted average shares outstanding	371,152	406,568	406,354	409,250

	<u>1st Quarter</u>	<u>2nd Quarter</u>	<u>3rd Quarter</u>	<u>4th Quarter</u>
Year Ended December 31, 2004:				
Net sales	\$ 868,383	\$ 837,592	\$ 915,132	\$1,028,627
Gross profit	108,329	16,058	92,094	90,591
Operating loss	(187,695)	(337,491)	(61,674)	(15,118)
Net loss	(168,743)	(335,791)	(56,476)	(6,599)
Preferred stock dividends and accretion, net of gain on redemption of preferred stock	(2,789)	(2,790)	(2,792)	100,513
Net income (loss) attributable to common stockholders	(171,532)	(338,581)	(59,268)	93,914
Basic net income (loss) per share	(0.51)	(0.91)	(0.16)	0.25
Diluted net income (loss) per share	(0.51)	(0.91)	(0.16)	(0.02)
Basic weighted average shares outstanding	335,399	372,436	372,940	373,844
Diluted weighted average shares outstanding	335,399	372,436	372,940	398,958

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GATEWAY, INC.

NOTES TO CONSOLIDATED FINANCIAL STATEMENTS—(Continued)

13. Restructuring and Other Special Charges:

Gateway recorded \$0.5 million, \$13 million, and \$412 million in net restructuring, transformation and integration charges during 2006, 2005 and 2004, respectively, which are included in cost of goods sold and selling, general, and administrative expenses.

Gateway adopted restructuring plans in 2004 and prior years to, among other things, reduce its workforce and close certain facilities, including closing 264 retail stores, and consolidate facilities. Adjustments of \$1 million were recorded in 2006 primarily related to better than expected recovery on Gateway retail store lease buyouts. The following table summarizes the status of all remaining restructuring plans as of December 31, 2006 (in millions):

	<u>2006</u>	<u>2005</u>
Accrued, January 1	\$ 26	\$ 79
Charges	—	—
		19
Cash settlements	(12)	(42)
Non-cash settlements	—	—
		(17)
Adjustments	(1)	(13)
Accrued, December 31	<u>\$ 13</u>	<u>\$ 26</u>

For all restructuring plans, approximate future cash outflows of \$13 million, primarily lease liabilities on closed facilities, are exceeded by expected future cash inflows of \$15 million from related sublease recoveries and asset dispositions.

The following table outlines the anticipated future net cash inflows, including amounts included in the lease payment tables provided in Note 5, associated with all restructuring plans (in thousands):

<u>Years Ending December 31:</u>	
2007	\$(7,067)
2008	3,415
2009	1,426
2010	1,050
2011	<u>(552)</u>
Thereafter	—
Total accrued restructuring liability	<u>\$(1,728)</u>

14. Related Party Transactions:

Through its acquisition of eMachines, Gateway acquired preferred stock in Alorica, Inc. that is convertible into approximately 17% of the common stock of Alorica, a company that provides reverse logistics, product registration, technical support, parts sales, PC refurbishing, software development, and other related services to Gateway and its customers. Between April 2004 and May 2005, the majority common stock shareholder of Alorica, Andy Lee, was employed as Gateway's Senior Vice President of Information Technology/Web. Gateway implemented additional procedures to provide for independent senior management review of any commercial relationships between Gateway and Alorica. Gateway paid approximately \$45 million, \$54 million, and \$43 million for the services described above during the years ended December 31, 2006, 2005, and 2004, respectively.

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GATEWAY, INC.

NOTES TO CONSOLIDATED FINANCIAL STATEMENTS—(Continued)

15. Subsequent Events:

On February 13, 2007, Gateway received notification from Revenue Ireland, the Irish taxing authority, that it had waived all further consideration related to possible capital gains treatment resulting from the dissolution and liquidation of certain Gateway entities in Europe. These entities ceased operations in 2001 and have been in the process of liquidation since then. Based on this notification, Gateway reduced its income taxes payable and increased the related income tax benefit as of and for the year ended December 31, 2006 by \$2.7 million.

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GATEWAY, INC.
VALUATION AND QUALIFYING ACCOUNTS
For the years ended December 31, 2006, 2005 and 2004
(in thousands)

	<u>Balance at Beginning of Period</u>	<u>Additions Charged to Expense</u>	<u>Deductions from Allowance</u>	<u>Balance at End of Period</u>
<i>Year ended December 31, 2004:</i>				
Allowance for uncollectible accounts receivable	\$ 9,526	\$ 11,333	\$(15,746)	\$ 5,113
<i>Year ended December 31, 2005:</i>				
Allowance for uncollectible accounts receivable	\$ 5,113	\$ 5,552	\$ (4,573)	\$ 6,092
<i>Year ended December 31, 2006:</i>				
Allowance for uncollectible accounts receivable	\$ 6,092	\$ 2,560	\$ (6,434)	\$ 2,218

Item 9. *Changes in and Disagreements with Independent Registered Public Accounting Firm on Accounting and Financial Disclosure*

None

Item 9A. *Controls and Procedures*

Evaluation of Disclosure Controls and Procedures

We evaluated the design and operating effectiveness of our disclosure controls and procedures as of December 31, 2006, pursuant to Rule 13a-15(b) of the Securities Exchange Act of 1934, as amended (the "Securities Exchange Act"). Based on this evaluation, our Chief Executive Officer and Chief Financial Officer concluded that, because of the material weakness in our internal control over financial reporting described below, our disclosure controls and procedures as defined in Rule 13a-15(e) were not effective. Notwithstanding the material weakness in our internal control over financial reporting as of December 31, 2006 described below, we believe that the consolidated financial statements contained in this report present fairly our financial condition, results of operations, and cash flows for the fiscal years covered thereby in all material respects. To address the material weakness in our internal control over financial reporting described below, management performed additional manual procedures and analysis and other post-closing procedures in order to prepare the consolidated financial statements included in this Annual Report on Form 10-K.

Management's Report on Internal Control Over Financial Reporting

Management is responsible for establishing and maintaining an adequate system of internal control over financial reporting, pursuant to Rule 13a-15(c) of the Securities Exchange Act, in order to provide reasonable assurance regarding the reliability of financial reporting and the preparation of financial statements for external purposes in accordance with accounting principles generally accepted in the United States ("GAAP"). A company's internal control over financial reporting includes policies and procedures that: (i) pertain to the maintenance of records that, in reasonable detail, accurately and fairly reflect the transactions and dispositions of the assets of the company, (ii) provide reasonable assurance that transactions are recorded as necessary to permit preparation of financial statements in accordance with accounting principles generally accepted in the United States, and that receipts and expenditures of the company are being made only in accordance with authorizations of management and directors of the company, and (iii) provide reasonable assurance regarding prevention or timely detection of unauthorized acquisition, use or disposition of the company's assets that could have a material effect on the financial statements.

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In accordance with the internal control reporting requirements of the Securities and Exchange Commission, management completed an assessment of the effectiveness of our internal control over financial reporting as of December 31, 2006. In making this assessment, management used the criteria set forth in the Internal Control—Integrated Framework by the Committee of Sponsoring Organizations of the Treadway Commission (“COSO”). The COSO framework summarizes each of the components of a company’s internal control system, including the: (i) control environment, (ii) risk assessment, (iii) information and communication, and (iv) monitoring (collectively, the “entity-level controls”), as well as (v) a company’s control activities (“process-level controls”). Management’s evaluation of the design and operating effectiveness of our internal controls over financial reporting identified a material weakness resulting from design deficiencies in the internal control system related to the recording of liabilities, receivables from suppliers and component inventory. A “material weakness” is defined as a significant deficiency or combination of significant deficiencies, that results in more than a remote likelihood that a material misstatement of the annual or interim financial statements will not be prevented or detected.

Specifically, during the course of the year-end close process, management examined our processes relating to our receipt of components from original equipment manufacturers (OEMs) and sale of components to original design manufacturers (ODMs). As a result of that evaluation, management concluded that we did not adequately design controls to ensure the timely accrual of liabilities to OEMs, recording of receivables from ODMs and receipt of inventory through; (a) timely reconciliation of open purchase orders to OEMs with inventory delivered to ODMs, and (b) timely review and resolution of discrepancies between OEM invoices and ODM receiving data. As a result of these deficiencies, management posted a material closing adjustment to the balance sheet as of December 31, 2006.

In addition to posting the appropriate adjustment, management also is taking the following steps to remediate this material weakness in 2007:

- Structural and operational review of current procurement and receiving procedures.
- Review and re-design of process level controls in Gateway’s procurement, receiving and accounts payable functions.
- Weekly review and comparison of OEM shipment reports to the open purchase order report.
- Monthly review and follow-up by accounting management to ensure appropriate reconciliation and accrual of un-vouchered invoices as required at period-end.
- Assessment and adjustment of current staffing in accounting and operational areas as necessary.

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Report of Independent Registered Public Accounting Firm

To the Board of Directors and Stockholders of Gateway, Inc.

We have audited management's assessment, included in the accompanying Management's Report on Internal Control Over Financial Reporting, appearing in Item 9a, that Gateway, Inc. and subsidiaries (the "Company") did not maintain effective internal control over financial reporting as of December 31, 2006, because of the effect of the material weakness identified in management's assessment based on criteria established in Internal Control—Integrated Framework issued by the Committee of Sponsoring Organizations of the Treadway Commission ("COSO"). The Company's management is responsible for maintaining effective internal control over financial reporting and for its assessment of the effectiveness of internal control over financial reporting. Our responsibility is to express an opinion on management's assessment and an opinion on the effectiveness of the Company's internal control over financial reporting based on our audit.

We conducted our audit in accordance with the standards of the Public Company Accounting Oversight Board (United States). Those standards require that we plan and perform the audit to obtain reasonable assurance about whether effective internal control over financial reporting was maintained in all material respects. Our audit included obtaining an understanding of internal control over financial reporting, evaluating management's assessment, testing and evaluating the design and operating effectiveness of internal control, and performing such other procedures as we considered necessary in the circumstances. We believe that our audit provides a reasonable basis for our opinions.

A company's internal control over financial reporting is a process designed by, or under the supervision of, the company's principal executive and principal financial officers, or persons performing similar functions, and effected by the company's board of directors, management, and other personnel to provide reasonable assurance regarding the reliability of financial reporting and the preparation of financial statements for external purposes in accordance with generally accepted accounting principles. A company's internal control over financial reporting includes those policies and procedures that (1) pertain to the maintenance of records that, in reasonable detail, accurately and fairly reflect the transactions and dispositions of the assets of the company; (2) provide reasonable assurance that transactions are recorded as necessary to permit preparation of financial statements in accordance with generally accepted accounting principles, and that receipts and expenditures of the company are being made only in accordance with authorizations of management and directors of the company; and (3) provide reasonable assurance regarding prevention or timely detection of unauthorized acquisition, use, or disposition of the company's assets that could have a material effect on the financial statements.

Because of the inherent limitations of internal control over financial reporting, including the possibility of collusion or improper management override of controls, material misstatements due to error or fraud may not be prevented or detected on a timely basis. Also, projections of any evaluation of the effectiveness of the internal control over financial reporting to future periods are subject to the risk that the controls may become inadequate because of changes in conditions, or that the degree of compliance with the policies or procedures may deteriorate.

A material weakness is a significant deficiency, or combination of significant deficiencies, that results in more than a remote likelihood that a material misstatement of the annual or interim financial statements will not be prevented or detected. The following material weakness has been identified and included in management's assessment:

During the course of the year-end close process, Gateway's management identified and concluded that in its receiving and selling of components with original design manufacturers, they did not adequately design controls to ensure the timely accrual of liabilities, recording of receivables from suppliers and receipt of inventory. As a result of these deficiencies, management posted a material closing adjustment to the balance sheet as of December 31, 2006.

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This material weakness was considered in determining the nature, timing, and extent of audit tests applied in our audit of the consolidated financial statements as of and for the year ended December 31, 2006, of the Company and this report does not affect our report on such consolidated financial statements.

In our opinion, management's assessment that the Company did not maintain effective internal control over financial reporting as of December 31, 2006, is fairly stated, in all material respects, based on the criteria established in Internal Control—Integrated Framework issued by the Committee of Sponsoring Organizations of the Treadway Commission. Also in our opinion, because of the effect of the material weakness described above on the achievement of the objectives of the control criteria, the Company has not maintained effective internal control over financial reporting as of December 31, 2006, based on the criteria established in Internal Control—Integrated Framework issued by the Committee of Sponsoring Organizations of the Treadway Commission.

We have also audited, in accordance with the standards of the Public Company Accounting Oversight Board (United States), the consolidated financial statements and financial statement schedule as of and for the year ended December 31, 2006, of the Company and our report dated February 23, 2007 expressed an unqualified opinion on those financial statements.

/s/ DELOITTE & TOUCHE LLP

Costa Mesa, California
February 23, 2007

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Item 9B. Other Information

None.

PART III

Item 10. Directors and Executive Officers of the Registrant

Information regarding our directors and executive officers is to be incorporated by reference from Gateway's 2007 Proxy Statement, which is to be filed with the Securities Exchange Commission not later than April 30, 2007 (120 days after the end of the fiscal year covered by this Form 10-K).

Item 11. Executive Compensation

Information regarding the compensation of our directors and executive officers is to be incorporated by reference from Gateway's 2007 Proxy Statement, which is to be filed with the Securities Exchange Commission not later than April 30, 2007 (120 days after the end of the fiscal year covered by this Form 10-K).

Item 12. Security Ownership of Certain Beneficial Owners and Management and Related Stockholder Matters

Information regarding ownership of our common stock by certain persons and equity compensation plan information is to be incorporated by reference from Gateway's 2006 Proxy Statement, which is to be filed with the Securities Exchange Commission not later than April 30, 2007 (120 days after the end of the fiscal year covered by this Form 10-K).

EQUITY COMPENSATION PLAN INFORMATION

The following table summarizes information, as of December 31, 2006, relating to equity compensation plans of Gateway pursuant to which grants of options, warrants or other rights to acquire shares may be granted from time to time.

Plan category	(a) Number of securities to be issued upon exercise of outstanding options, warrants and rights (in millions)	(b) Weighted-average exercise price of outstanding options, warrants and rights	(c) Number of securities remaining available for future issuance under equity compensation plans (in millions, excluding securities reflected in column (a))
Equity compensation plans approved by security holders(1)	38.0	\$ 7.56	40.5
Equity compensation plans not approved by security holders(2)	0.4	\$ 56.72	
Total	38.4	\$ 8.04	40.5

- (1) These plans are Gateway's 1996 Non-Employee Director Stock Option Plan, 1996 Long-Term Incentive Equity Plan and 2000 Equity Incentive Plan.
- (2) Gateway's sole equity compensation plan not previously submitted to stockholders for approval is our 2000 Employee Equity Incentive Plan, which was only used as an interim vehicle prior to the submission of our 2000 Equity Incentive Plan for stockholder approval. The 2000 Employee Equity Incentive Plan, which covered approximately 800,000 common stock shares at a weighted average exercise price of \$56.67, was terminated upon receiving such stockholder approval.

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Item 13. *Certain Relationships and Related Transactions*

Information regarding relationships or transactions between our affiliates and us is to be incorporated by reference from Gateway's 2007 Proxy Statement, which is to be filed with the Securities Exchange Commission not later than April 30, 2007 (120 days after the end of the fiscal year covered by this Form 10-K).

Item 14. *Principal Accountant Fees and Services*

Information regarding principal accountant fees and services is to be incorporated by reference from Gateway's 2007 Proxy Statement, which is to be filed with the Securities Exchange Commission not later than April 30, 2007 (120 days after the end of the fiscal year covered by this Form 10-K).

Table of Contents**PART IV****Item 15. Exhibits and Financial Statement Schedules**

(a) The following documents are filed as a part of this Report:

(1) Financial Statements and Financial Statement Schedule. See Index to Consolidated Financial Statements and Financial Statement Schedule at Item 8 of this Annual Report.

(2) Exhibits. Exhibits identified below as on file with the Securities and Exchange Commission are incorporated herein by reference as exhibits hereto.

Exhibit Number	Exhibit Description	Incorporated by Reference		
		Form	Exhibit (s)	Filing Date
2.1	Agreement and Plan of Merger, dated as of January 30, 2004, by and among Gateway, Inc., Gateway Sub, LLC, Gateway Sub II, LLC and EM Holdings, Inc.	8-K	2.1	February 3, 2004
3.1	Restated Certificate of Incorporation of Gateway, Inc., as amended	10-K	3.1	February 12, 2002
3.2	Amended and Restated Bylaws of Gateway, Inc.	8-K	3.2	December 11, 2006
4.1	Rights Agreement, dated as of January 19, 2000, between Gateway, Inc. and UMB Bank, N.A., as Rights Agent, including all exhibits thereto.	8-A	1.0	February 4, 2000
4.2	Registration Agreement dated February 22, 1991 between Gateway, Inc., Theodore W. Waitt and Norman W. Waitt, Jr. as the sole trustee and sole beneficiary of the Norman W. Waitt, Jr. S Corp. Trust, together with Amendment No. 1 to the Registration Agreement dated as of October 19, 1993*	S-1	10.11	October 21, 1993
4.3	Form of Stockholders' and Registration Rights Agreement, by and among Gateway, Inc., Mr. Lap Shun (John) Hui and certain Gateway, Inc. stock recipients	8-K	2.1	February 3, 2004 (Exhibit B within Exhibit 2.1)
4.4	Registration Rights Agreement, dated as of March 22, 2005, between Theodore W. Waitt and Gateway, Inc.	8-K	10.1	March 25, 2005
4.5	Indenture between Gateway, Inc. and U.S. Bank National Association, as Trustee (including form of 1.50% Senior Convertible Notes due 2009 and form of 2.00% Senior Convertible Notes due 2011), dated as of December 21, 2004	8-K	10.1	December 21, 2004
10.1	Tax Indemnification Agreement, dated as of December 6, 1993 between Gateway, Inc., and Theodore W. Waitt and the Norman W. Waitt, Jr. S Corp. Trust.*	10-K	10.1	March 31, 1994
10.2	Indemnification Agreement dated as of December 6, 1994 between Gateway, Inc., and Theodore W. Waitt.*	10-K	10.2	March 31, 1995

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Exhibit Number	Exhibit Description	Incorporated by Reference		
		Form	Exhibit (s)	Filing Date
10.3	Gateway, Inc. 1996 Long-Term Incentive Equity Plan, as amended and restated*	10-K	10.7	March 5, 2001
10.4	Gateway, Inc. 2000 Equity Incentive Plan, as amended and restated*	10-Q	10.18	August 14, 2000
10.5	Gateway, Inc. 1996 Non-Employee Directors Stock Option Plan as amended.*	10-Q	10.20	August 14, 1998
10.6	Form of Gateway, Inc. Restricted Stock Grant Notice*	10-Q	10.2	November 8, 2005
10.7	Gateway, Inc. Management Incentive Plan, as amended*	10-Q	10.10	July 24, 2001
10.8	Change in Control Compensation Plan, as amended*	10-K	10.12	April 15, 2003
10.9	Non-Competition Agreement, dated as of January 30, 2004, by and between Mr. Lap Shun (John) Hui and Gateway, Inc.	10-K	10.18	February 27, 2004
10.10	Non-Competition Agreement, dated as of January 30, 2004, by and between Mr. Wayne R. Inouye and Gateway, Inc.*	10-K	10.19	February 27, 2004
10.11	Credit Agreement dated October 30, 2004, among Gateway, Inc., Gateway Professional LLC, Gateway Manufacturing LLC, eMachines, Inc.; other Credit Parties signing the Credit Agreement; General Electric Capital Corporation; and other Lenders signing the Credit Agreement	8-K	10.1	November 2, 2004
10.12	Amendment No. 2 dated June 28, 2006 to Credit Agreement, dated October 30, 2004, among Gateway, Inc., Gateway Professional LLC, Gateway Manufacturing LLC, Gateway US Retail, Inc., and General Electric Capital Corporation, as agent and lender	8-K	10.1	June 30, 2006
10.13	Amendment No. 3 dated December 26, 2006 to Credit Agreement, dated October 30, 2004, among Gateway, Inc., Gateway Professional LLC, Gateway Manufacturing LLC, Gateway US Retail, Inc., and General Electric Capital Corporation, as agent and lender	8-K	10.1	January 3, 2007
10.14	Stock Purchase Agreement between America Online, Inc. and Gateway, Inc. dated as of November 1, 2004	8-K	10.1	November 5, 2004
10.15	Stock Transfers and Future Payments Agreement between America Online, Inc. and Gateway, Inc. dated as of November 1, 2004	8-K	10.2	November 5, 2004
10.16	Marketing, Development and Settlement Agreement, dated as of April 7, 2005, by and between Microsoft Corporation and Gateway, Inc.	10-Q	10.1	August 15, 2005

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Exhibit Number	Exhibit Description	Incorporated by Reference		
		Form	Exhibit (s)	Filing Date
10.17	Employment Offer Agreement, dated as of April 26, 2006, by and between Richard D. Snyder and Gateway, Inc.*	8-K	10.1	April 27, 2006
10.18	Stock Option Agreement, dated as of April 26, 2006, by and between Richard D. Snyder and Gateway, Inc.*	8-K	10.2	April 27, 2006
10.19	Separation Agreement, effective as of April 30, 2006, by and between Scott Bauhofer and Gateway, Inc.*	8-K	10.1	April 28, 2006
10.20	Separation Agreement, effective as of April 29, 2006, by and between Bruce Smith and Gateway, Inc.*	8-K	10.2	April 28, 2006
10.21	Separation Agreement, effective as of February 8, 2006, by and between Wayne R. Inouye and Gateway, Inc.*	10-Q	10.1	May 9, 2006
10.22	Employment Offer Letter by and between J. Edward Coleman and Gateway, Inc., dated September 1, 2006*	8-K	10.1	September 7, 2006
10.23	Gateway, Inc. 2006 Change In Control Compensation Plan, effective as of September 29, 2006*	8-K	10.1	October 5, 2006
10.24	Form of Individual Change In Control Agreement*	8-K	10.2	October 5, 2006
10.25	Agreement, dated December 5, 2006, among Gateway, Inc., Scott Galloway and Firebrand Partners III, LLC, Harbinger Capital Partners Master Fund I, Ltd., and Harbinger Capital Partners Special Situations Fund, L.P. and its affiliates	8-K	10.1	December 11, 2006
21.1	List of subsidiaries			Filed herewith
23.1	Consent of Deloitte & Touche LLP			Filed herewith
24.1	Powers of attorney			Included herein on the signature page of this Annual Report on Form 10-K
31.1	Certification by CEO pursuant to Rule 13a-14(a) or 15d-14 (a), as adopted pursuant to Section 302 of the Sarbanes-Oxley Act of 2002.			Filed herewith
31.2	Certification by CFO pursuant to Rule 13a-14(a) or 15d-14 (a), as adopted pursuant to Section 302 of the Sarbanes-Oxley Act of 2002.			Filed herewith
32.1	Certification by CEO pursuant to 18 U.S.C. Section 1350, as adopted pursuant to Section 906 of the Sarbanes-Oxley Act of 2002.			Furnished herewith
32.2	Certification by CFO pursuant to 18 U.S.C. Section 1350, as adopted pursuant to Section 906 of the Sarbanes-Oxley Act of 2002.			Furnished herewith

* Indicates a management contract or compensatory plan.

Gateway will furnish upon request any exhibit described above upon payment of Gateway's reasonable expenses for furnishing such exhibit.

Table of Contents**SIGNATURES**

Pursuant to the requirements of Section 13 or 15(d) of the Securities Exchange Act of 1934, the Registrant has duly caused this report to be signed on its behalf by the undersigned, thereunto duly authorized, on February 23, 2007.

GATEWAY, INC.

By: /s/ JOHN P. GOLDSBERRY
John P. Goldsberry
 Senior Vice President and Chief Financial Officer -
 (Principal Financial Officer)

By: /s/ NEAL E. WEST
Neal E. West
 Vice President and Controller
 (Principal Accounting Officer)

Each person whose signature appears below constitutes and appoints John P. Goldsberry, Michael R. Tyler and Mark Dickey or any one of them, his attorney-in-fact, for such person in any and all capacities, to sign any amendments to this report and to file the same, with exhibits thereto, and other documents in connection therewith, with the Securities and Exchange Commission, hereby ratifying and confirming all that said attorneys-in-fact, or substitute or substitutes, may do or cause to be done by virtue hereof.

Pursuant to the requirements of the Securities Exchange Act of 1934, this report has been signed below by the following persons on behalf of the Registrant in the capacities indicated as of February 23, 2007:

<u>Signature</u>	<u>Title</u>
<u>/s/ J. EDWARD COLEMAN</u> J. Edward Coleman	Chief Executive Officer and Director (Principal Executive Officer)
<u>/s/ JOHN P. GOLDSBERRY</u> John P. Goldsberry	Senior Vice President and Chief Financial Officer (Principal Financial Officer)
<u>/s/ NEAL E. WEST</u> Neal E. West	Vice President and Controller (Principal Accounting Officer)
<u>/s/ QUINCY L. ALLEN</u> Quincy L. Allen	Director
<u>/s/ JANET M. CLARKE</u> Janet M. Clarke	Director
<u>/s/ SCOTT GALLOWAY</u> Scott Galloway	Director
<u>/s/ GEORGE H. KRAUSS</u> George H. Krauss	Director
<u>/s/ DOUGLAS L. LACEY</u> Douglas L. Lacey	Director

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Signature	Title
<u>/s/ JOSEPH G. PARHAM, JR.</u> Joseph G. Parham, Jr.	Director
<u>/s/ RICHARD D. SNYDER</u> Richard D. Snyder	Chairman of the Board
<u>/s/ PAUL E. WEAVER</u> Paul E. Weaver	Director